KTH Information and Communication Technology

IH1611 spring 2019

Problems to student recitation 6

1. Assume that half (50 %) of the transistors in a CMOS circuit have subthreshold slope (S) of 60 mV/decade and half of the transistors have S = 70 mV/decade. What is the off-state power, compared to a case where all of the transistors in the circuit have S = 65 mV/decade?

   EXTRA: What happens if S is uniformly distributed between 60 and 70 mV/decade?

2. What happens to the gate delay if the threshold voltage is raised by 100 mV (absolute value) for both NMOS and PMOS transistors in a CMOS circuit?

3. Explain how channel width is defined in FinFET technology and how larger widths can be achieved for PMOS devices in balanced CMOS inverters.

4. What are the main similarities for CMOS imaging arrays and memory circuits? Both SRAM and DRAM could be considered. What is the main difference in terms of layout density/cell design?

5. Explain the complete cell design for an imaging pixel that is color sensitive. Draw a cross-section of the pixel.

6. Both CMOS logic circuits and the three main memory types are charged based. Explain what this means for each case. What is the connection between charge and memory and logic states/levels that are sensed as voltages?