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OF TECHNOLOGY

Semiconductor Devices
Spring 2019

Lecture 11

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This Lecture

- Reading
- **L12** Feb 20 8-10 Q22 MOS-based memory devices and image sensors
  Ch. 6.16, Ch. 5.10 plus additional PDFs
- Concepts:
  - Image sensor arrays, CCD and MOSFETs, read-out
  - The three main types of seminconductor memory (SRM, DRAM, Flash)

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CCD – Charge coupled device

- CCD imager – large number of MOS capacitors packed in two-dimensional array
  - Collect packets of electrons generated by photons (visible light)
  - The physics at work is called ”deep depletion”
  - Transfer packets to charge sensing circuit in serial manner

Figure 5.28 Deep depletion. (a) Immediately after a gate voltage $V_g >$, V_t is applied, there are no electrons at the surface. (b) After exposure to light, photo-generated electrons have been collected at the surface. The number of electrons is proportional to the light intensity.

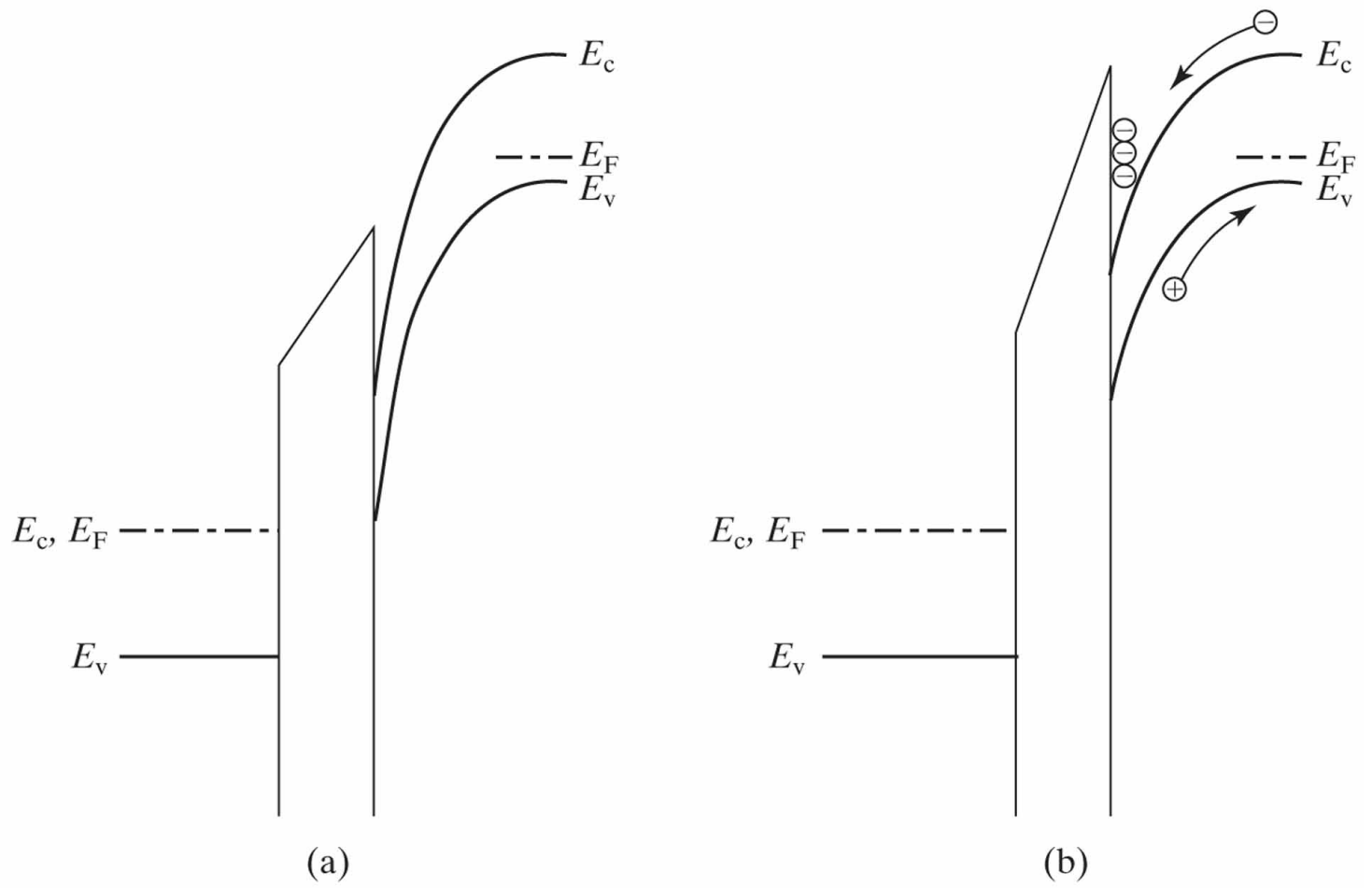


Figure 5.29 Deep-depletion C–V.

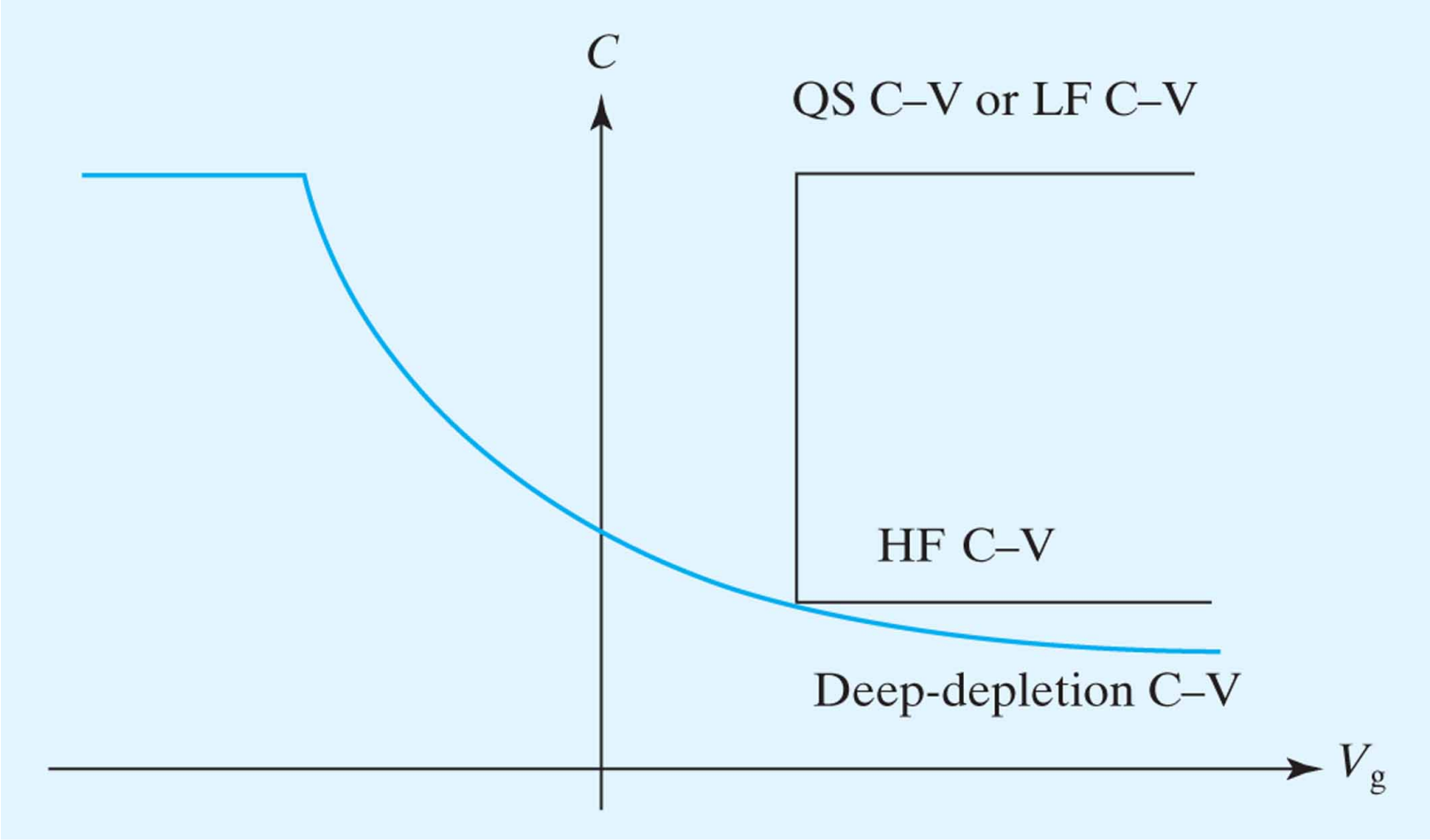
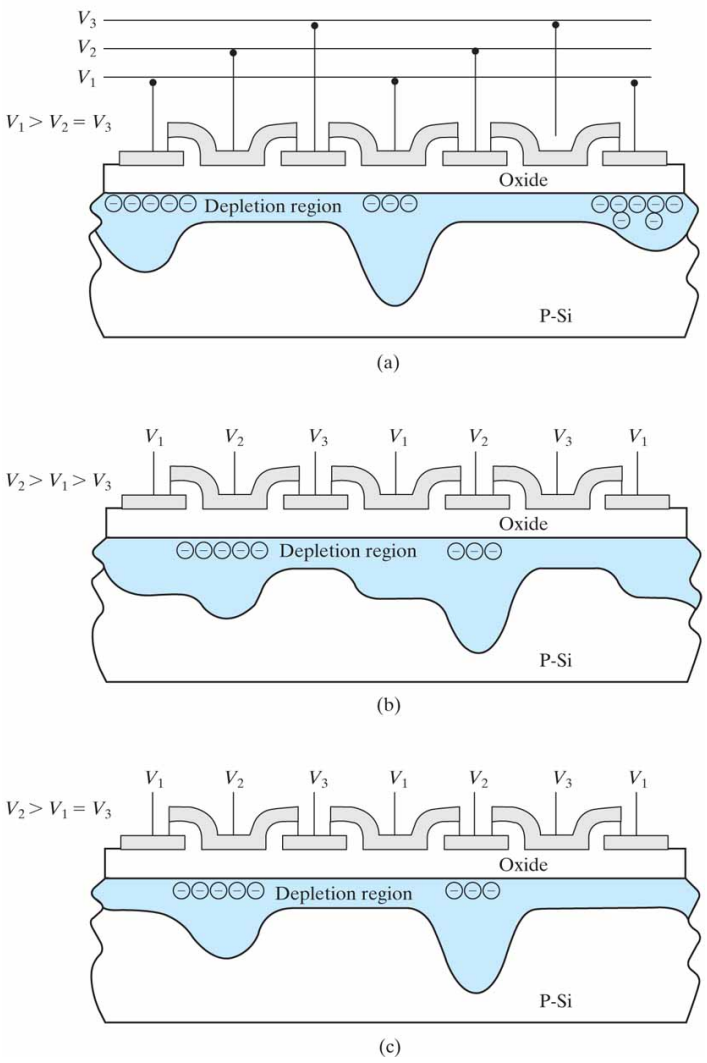


Figure 5.30 How CCD shifts the charge packets. The array is biased in the sequence (a), (b), (c), (a), (b), (c), (a) ... . The drawing in (c) is identical to (a) but with all the charge packets shifted to the right by one capacitor element.



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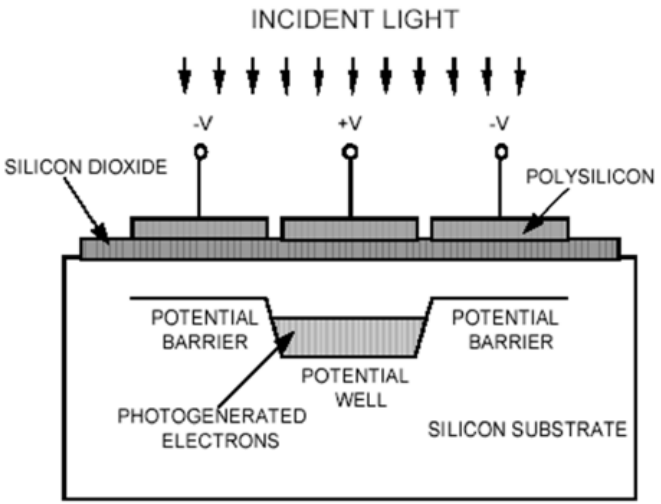
CCD charge transfer



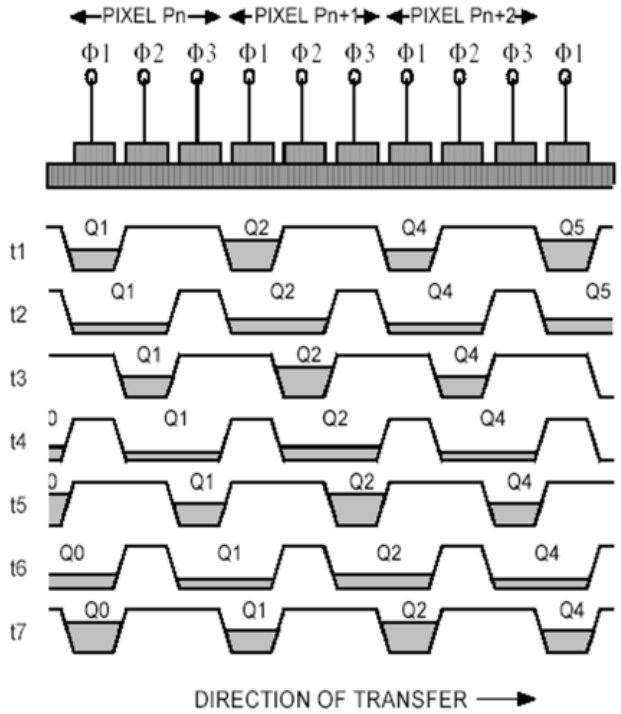
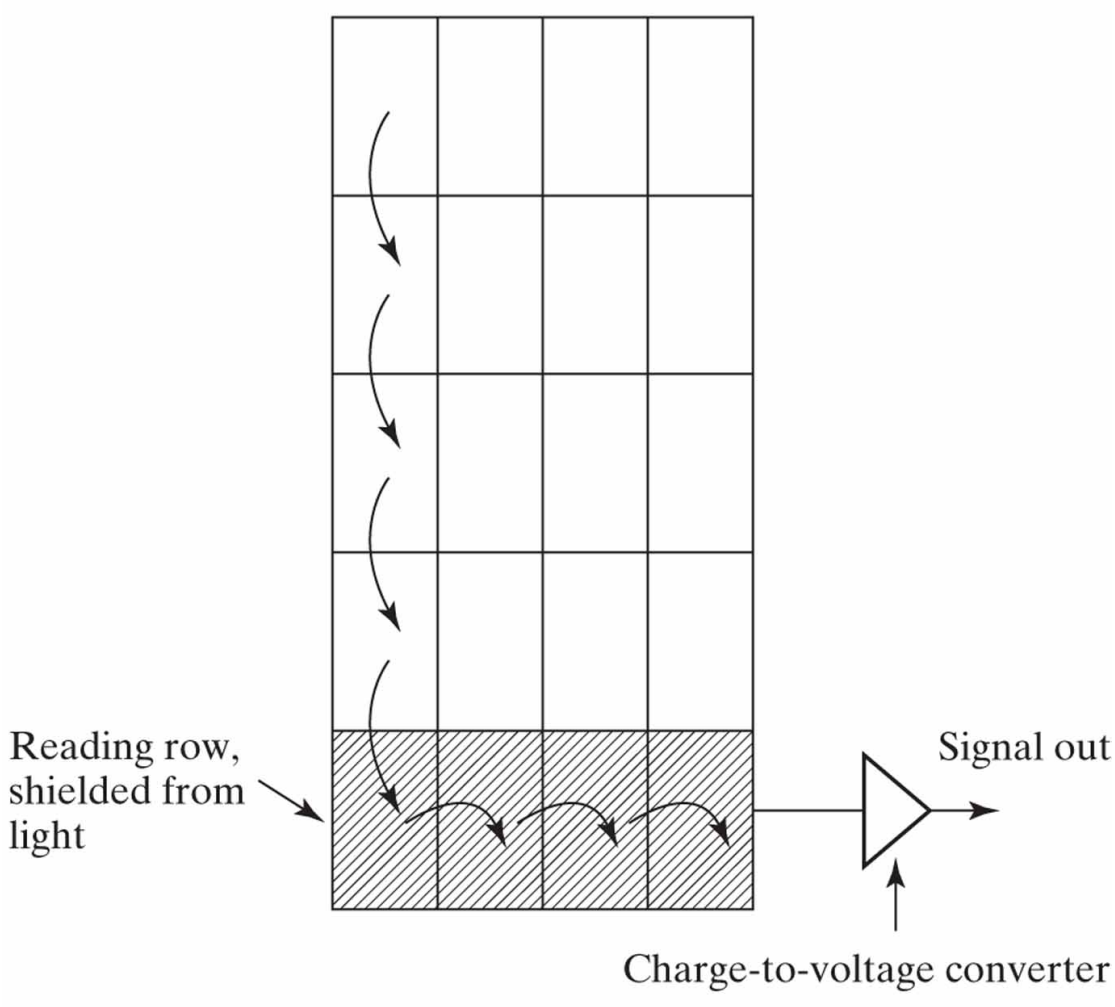


Figure 5.31 Architecture of a two-dimensional CCD imager. The arrows show the path of the charge-packet movement.



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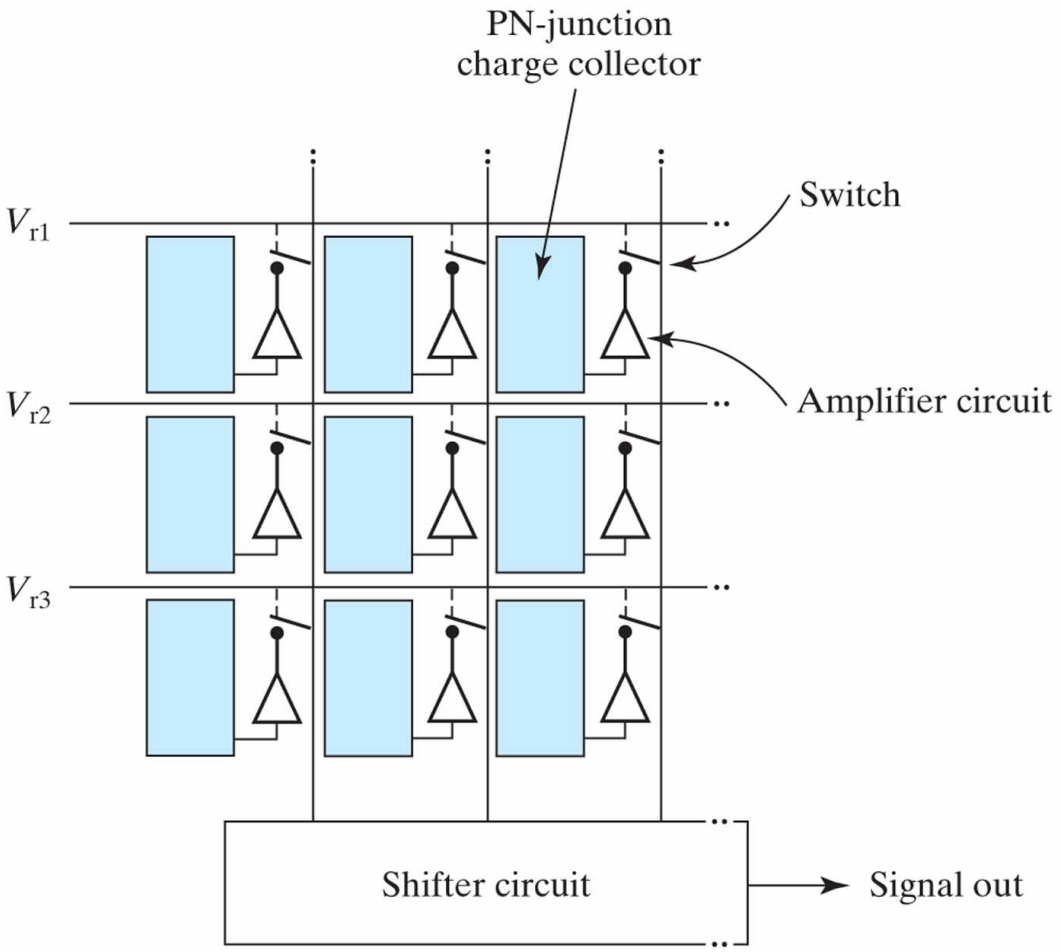
CMOS imager

- Open-circuit n+p-junction collect light generated charge (EHP)
- Pn-junction is capacitor and output voltage is connected to amplifier in each pixel

Figure 5.32 Architecture of a CMOS imager. Each array element has its own charge-to-voltage converter represented by the triangle. Actual imagers may support hundreds to over a thousand rows and columns of pixels.



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Pixel design

- Passive Pixel Sensor
  - 1 transistor per pixel
  - small pixel, large fill factor
  - but slow, low SNR

- Active Pixel Sensor
  - 3-4 transistors per pixel
  - fast, higher SNR, but
  - larger pixel, lower fill factor
  - 3 Tr structure, 4 Tr structure, photo gate structure

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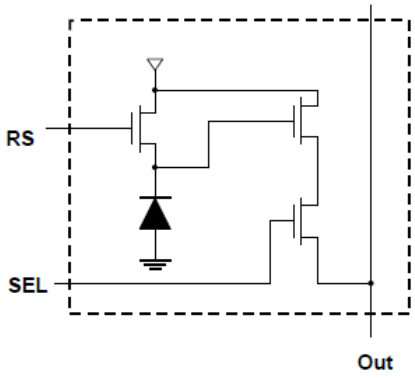
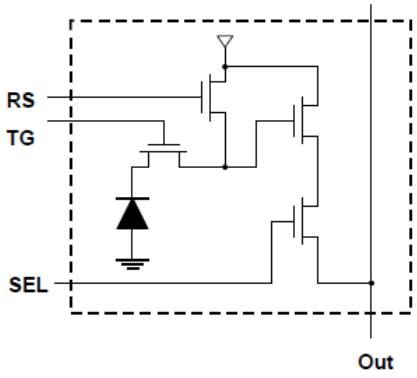
Active pixels



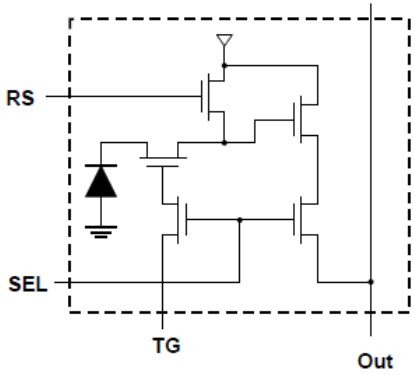
3-Tr Structure

- simple process
- high fill factor
- pixel reset noise
- low S/N



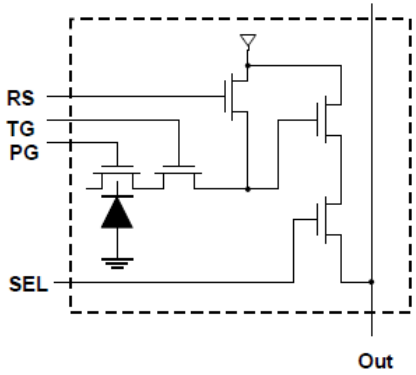
4-Tr Structure

- process for low shallow potential photodiode
- low fill factor
- low dark level
- higher sensitivity



5-Tr Structure

- 4-Tr + addressed readout
- full random access
- single CDS possible
- lowest fill factor



Photogate Structure

- simple process
- 4-Tr like operation
- signal charge shifting by PG & TG pulse
- additional signal line
- low blue response

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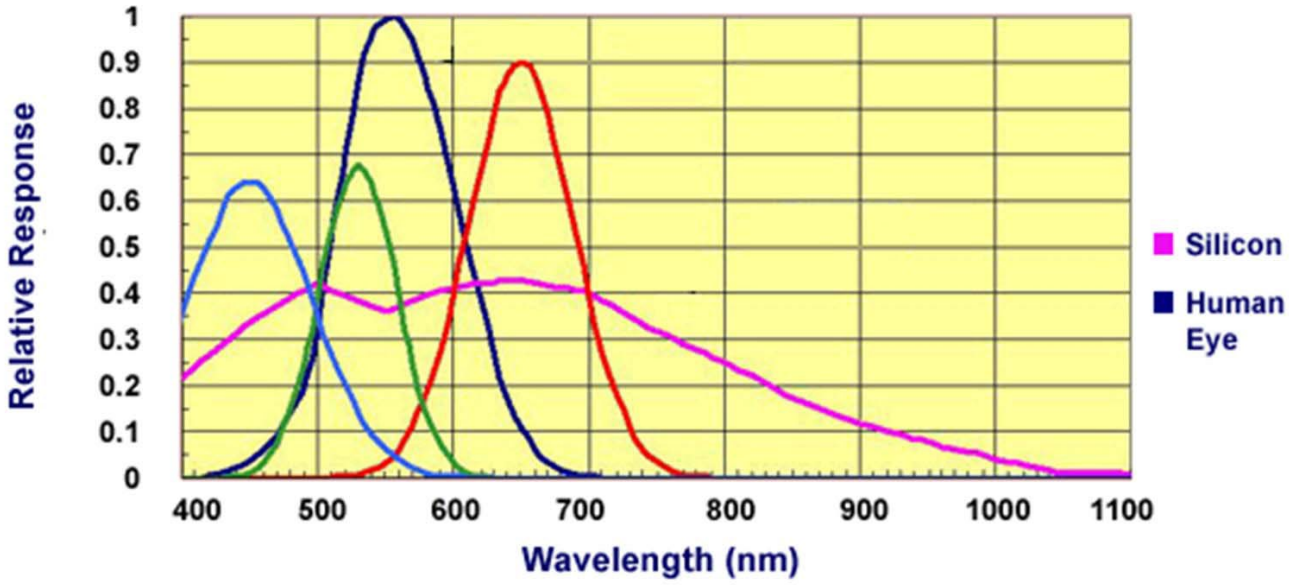
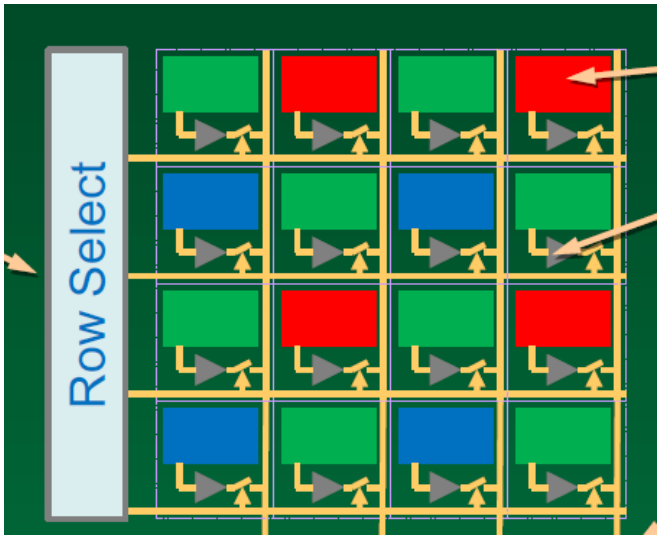
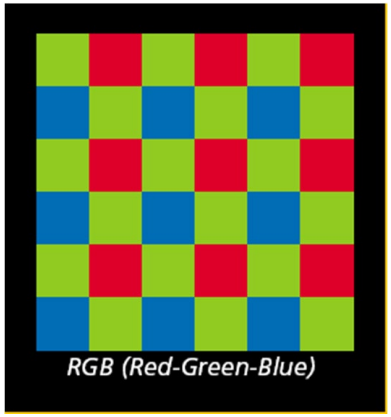
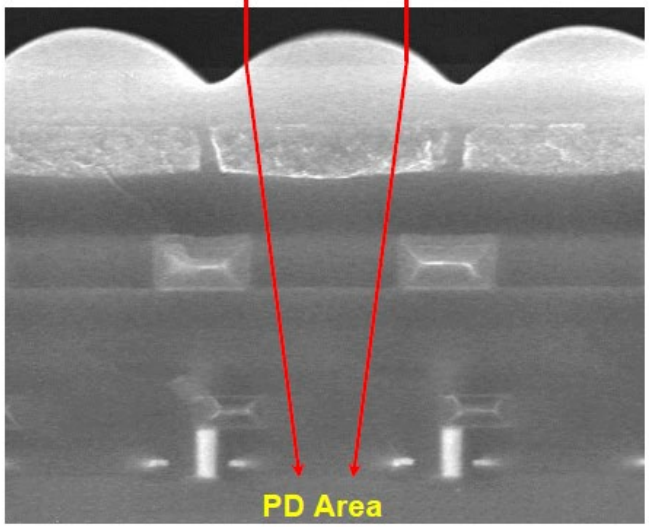
How to capture colors



How to capture colors







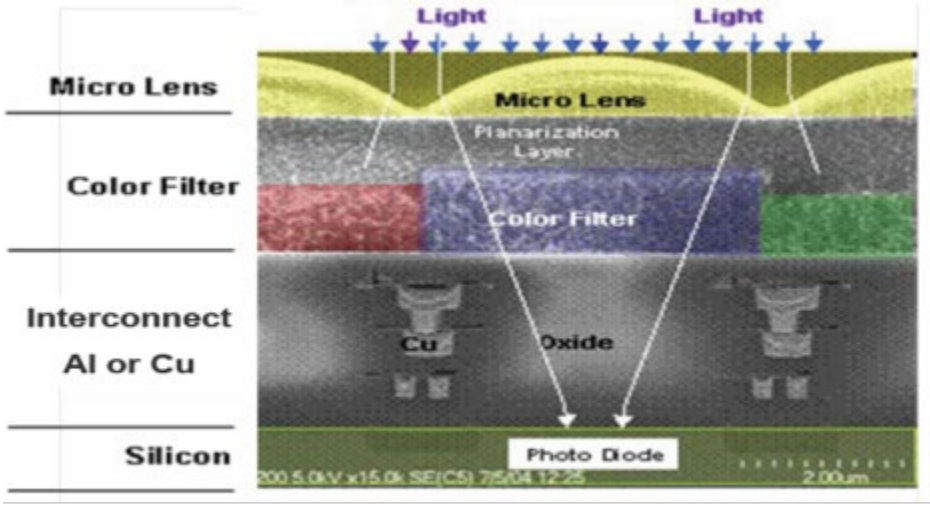
Micro Lens

Color Filter

Shield Metal Layer

MOS Transistors

Silicon Substrate



Source : IBM (FSI)

Figure 6.34 (a) Schematic of an SRAM cell. (b) Layout of a 32 nm technology SRAM. (From [16]. © 2007 IEEE.) The dark rectangles are the contacts. The four horizontal pieces are the gate electrodes and the two PFETs have larger Ws than the six NFETs. Metal interconnects (not shown) cross couple the two inverters.

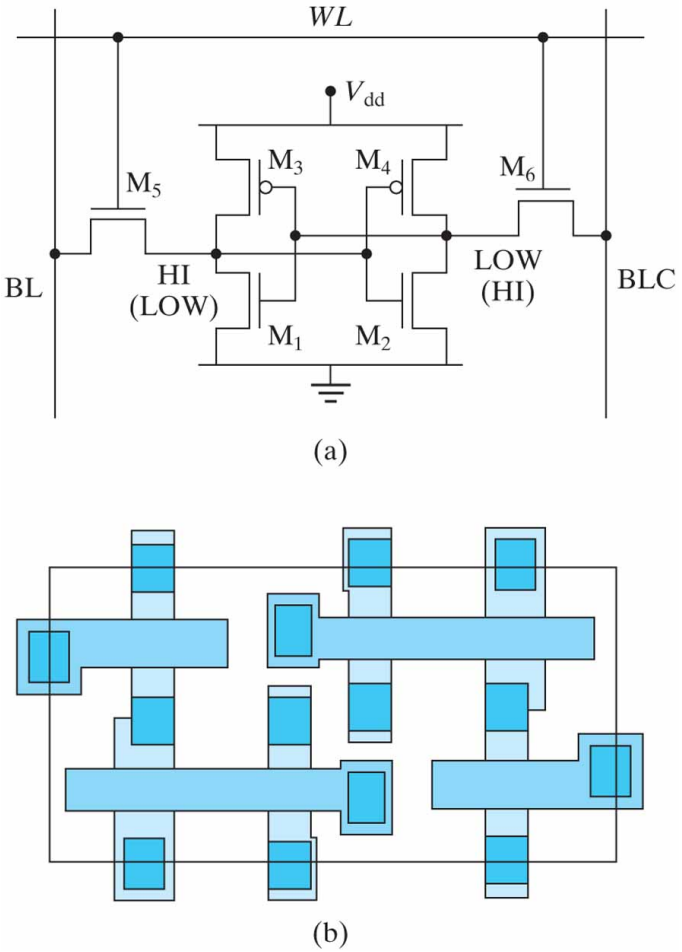


Table 6.1 The differences among three types of memories.

TABLE 6–1 • The differences among three types of memories.

	Keep Data Without Power?	Cell Size and Cost/bit	Rewrite Cycles	Write-One-byte Speed	Compatible with Basic CMOS Manufacturing	Main Applications
SRAM	No	Large	Unlimited	Fast	Totally	Embedded in logic chips
DRAM	No	Small	Unlimited	Fast	Need modifications	Stand-alone chips and embedded
Flash memory	Yes	Smallest	Limited	Slow	Need extensive modifications	Nonvolatile storage stand-alone

Figure 6.35 A schematic DRAM cell array. Each cell consists of a transistor and a capacitor.

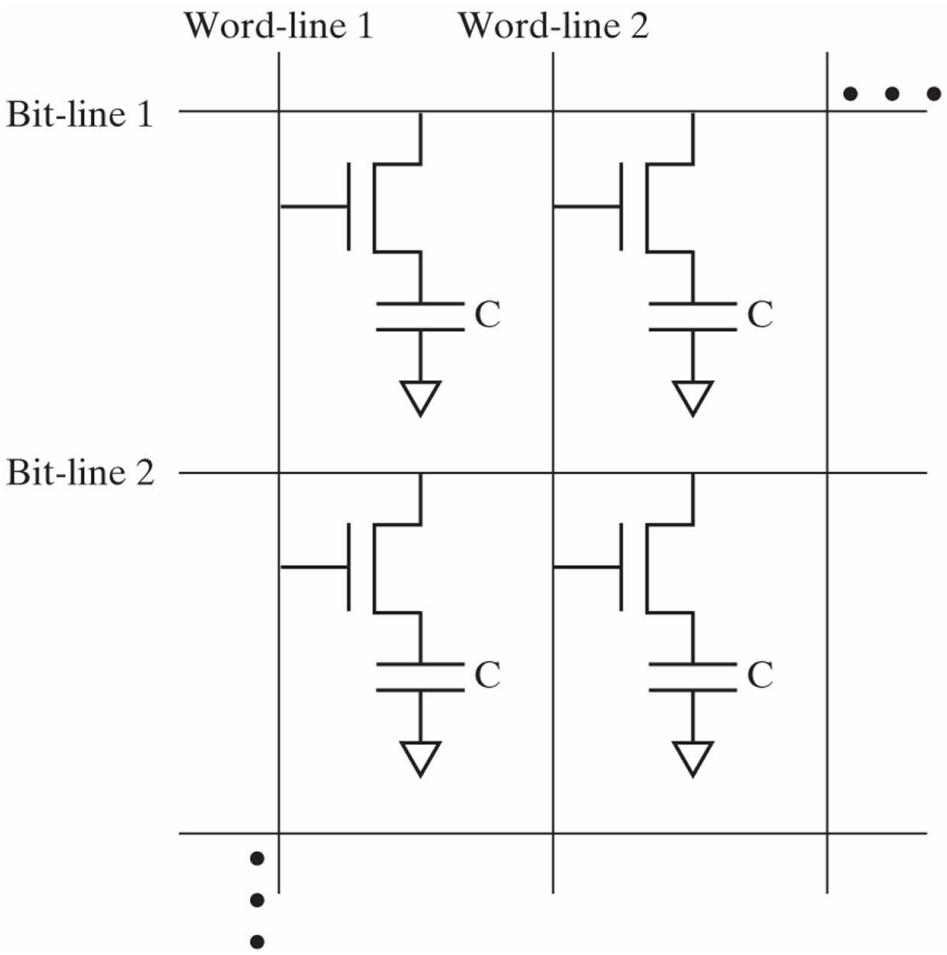
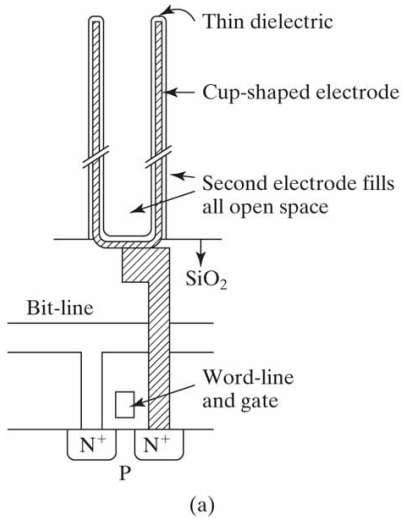
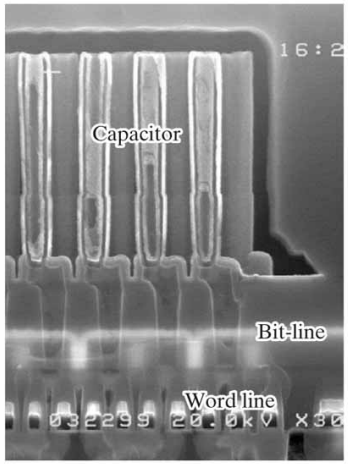


Figure 6.36 (a) Schematic drawing of a DRAM cell with a cup-shaped capacitor. (b) Cross-sectional image of DRAM cells. The capacitors are on top and the transistors are near the bottom. (From [17]. © 2002 IEEE.)

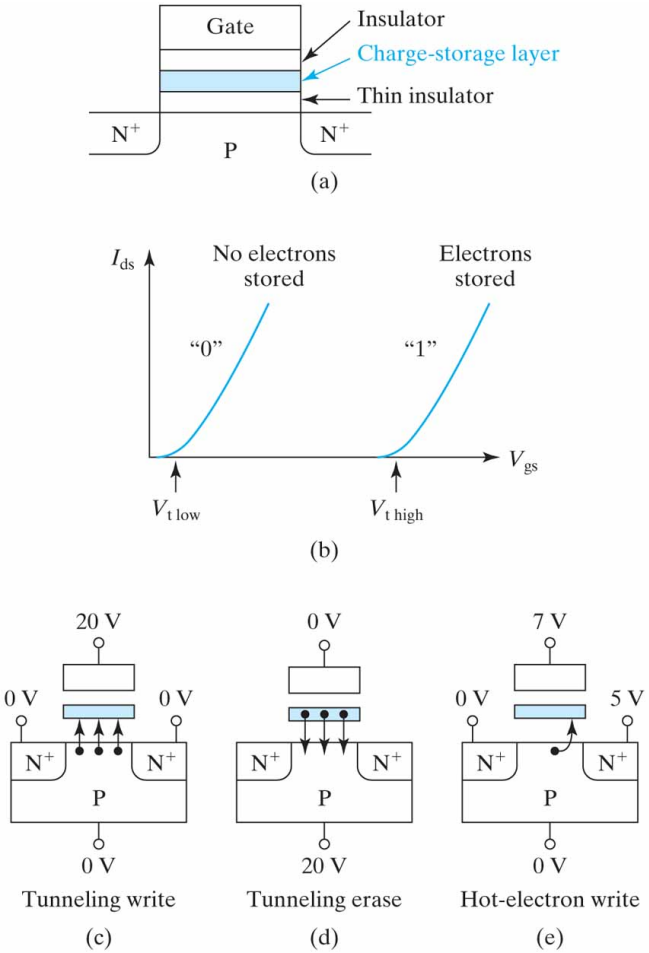


(a)



(b)

Figure 6.37 (a) A charge-storage NVM cell has a charge-storage layer in the gate dielectric stack; (b) V_t is modified by trapping electrons; (c) electron injection by tunneling; (d) electron removal by tunneling; and (e) electron injection by hot-electron injection.



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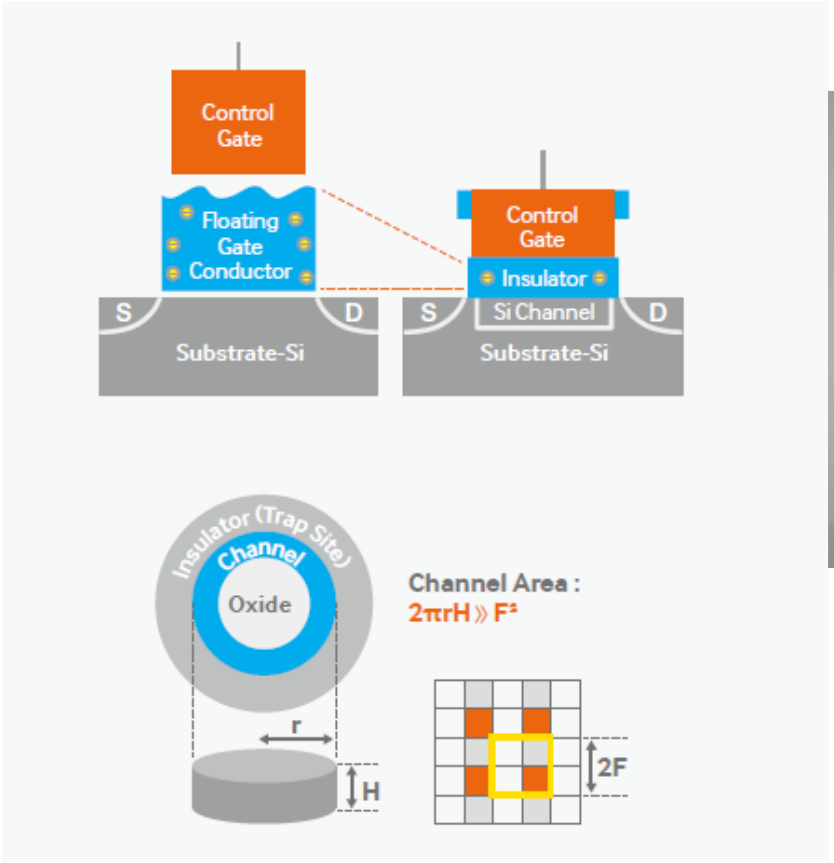
3D (vertical) NAND flash



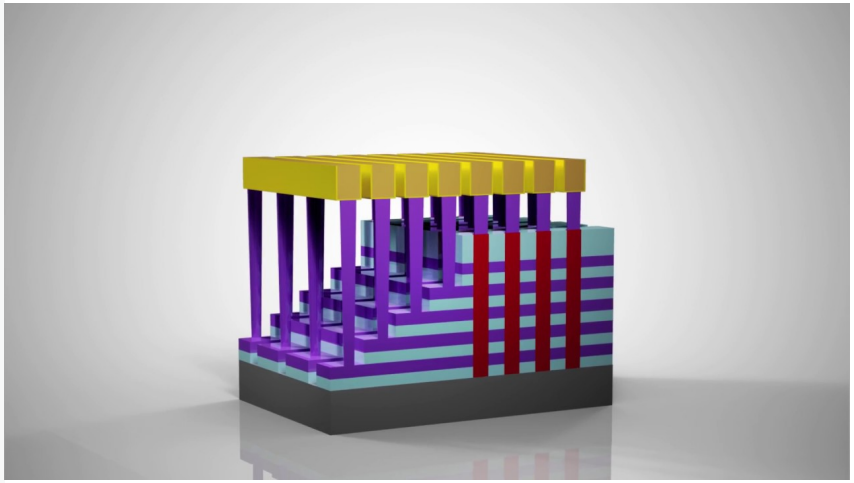


Figure 6.38 (a) Concept of a resistance-change memory such as a PCM. (b) Program the PCM into high-resistance state by rapid solidification, producing a highly resistive amorphous phase. (c) Program the PCM into low-resistance state by annealing, turning the amorphous material into a conductive crystalline phase.