ROYAL INSTITUTE
OF TECHNOLOGY

Semiconductor Devices
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Lecture 11

ROYAL INSTITUTE OF TECHNOLOGY

This Lecture

- Reading
  - Chapter 7 selected figures
  - Figs. 7-2, 7-5&7-6, 7-9, 7-13 & 7-14, 7-18 & 7-19
- Concepts:
  - MOFSET OFF-state, leakage
  - ION vs IOFF
  - Gate vs. Drain control of channel potential
  - Modern ultra-thin body and FinFETs

Figure 6.18 (a) CMOS inverter; (b) IV characteristics of NFET and PFET; and (c) $V_{out} = V_{dsN} = 2\text{ V} + V_{dsP}$ according to (a).

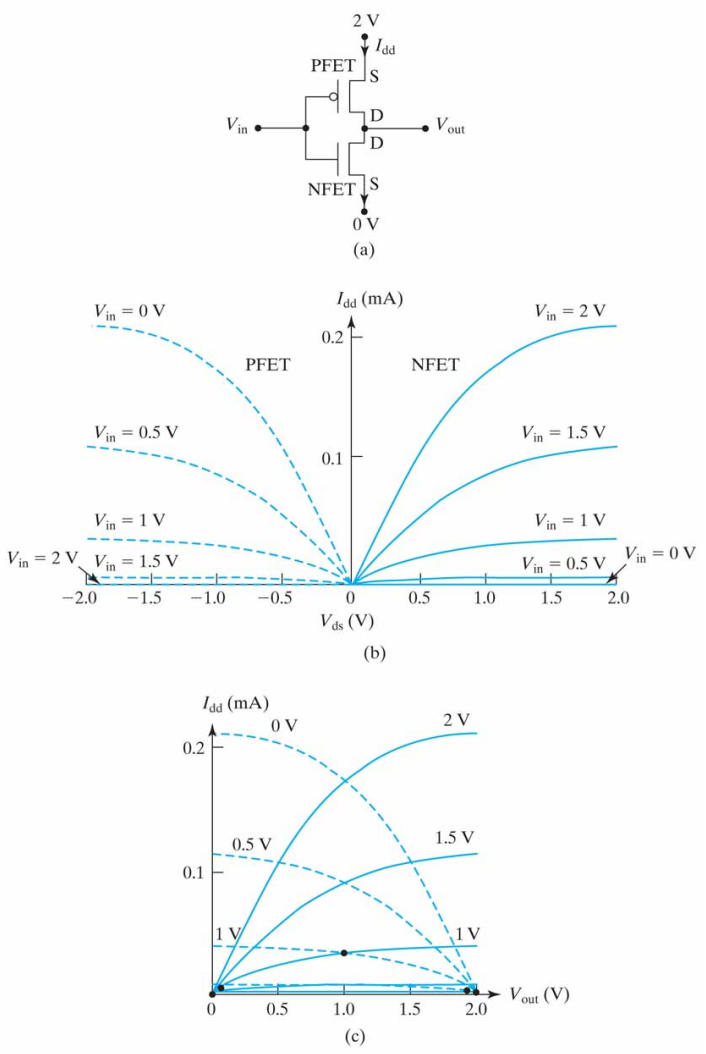

Figure 6.19 The VTC of a CMOS inverter.

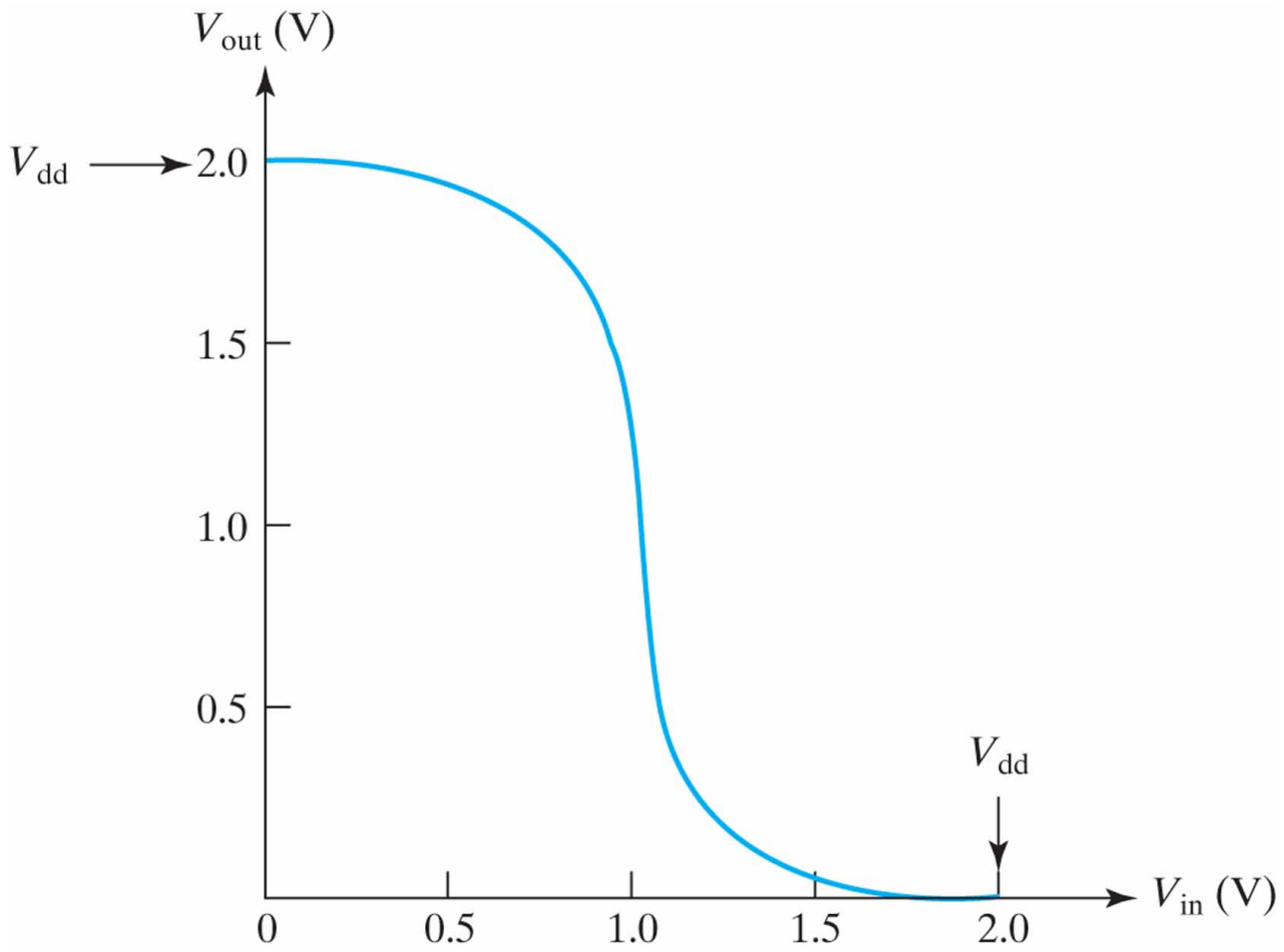

Figure 7.2 The current that flows at $V_{gs} < V_t$ is called the subthreshold current. $V_t \sim 0.2$ V. The lower/upper curves are for V_{ds} = 50 mV/1.2 V. After Ref. [2]. (b) When V_g is increased, E_c at the surface is pulled closer to E_F, causing n_s and I_{ds} to rise; (c) equivalent capacitance network; (d) subthreshold I-V with V_t and I_{off}. Swing, S, is the inverse of the slope in the subthreshold region.

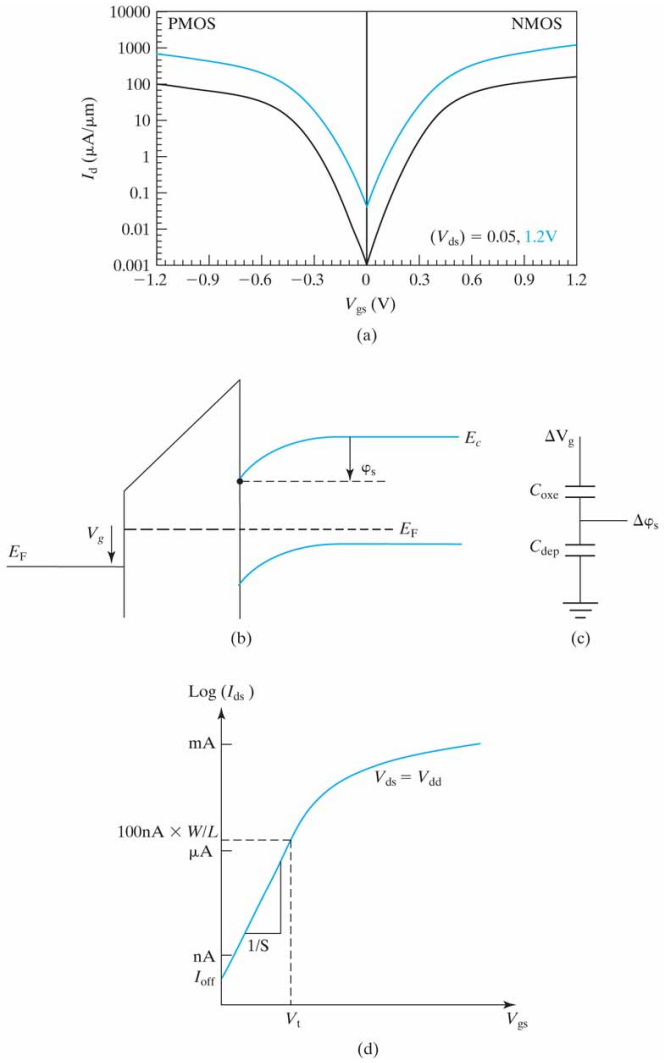

Figure 7.5 a–d: Energy band diagram from source to drain when V_{gs} = 0V and V_{gs} = V_t. a–b long channel; c–d short channel.

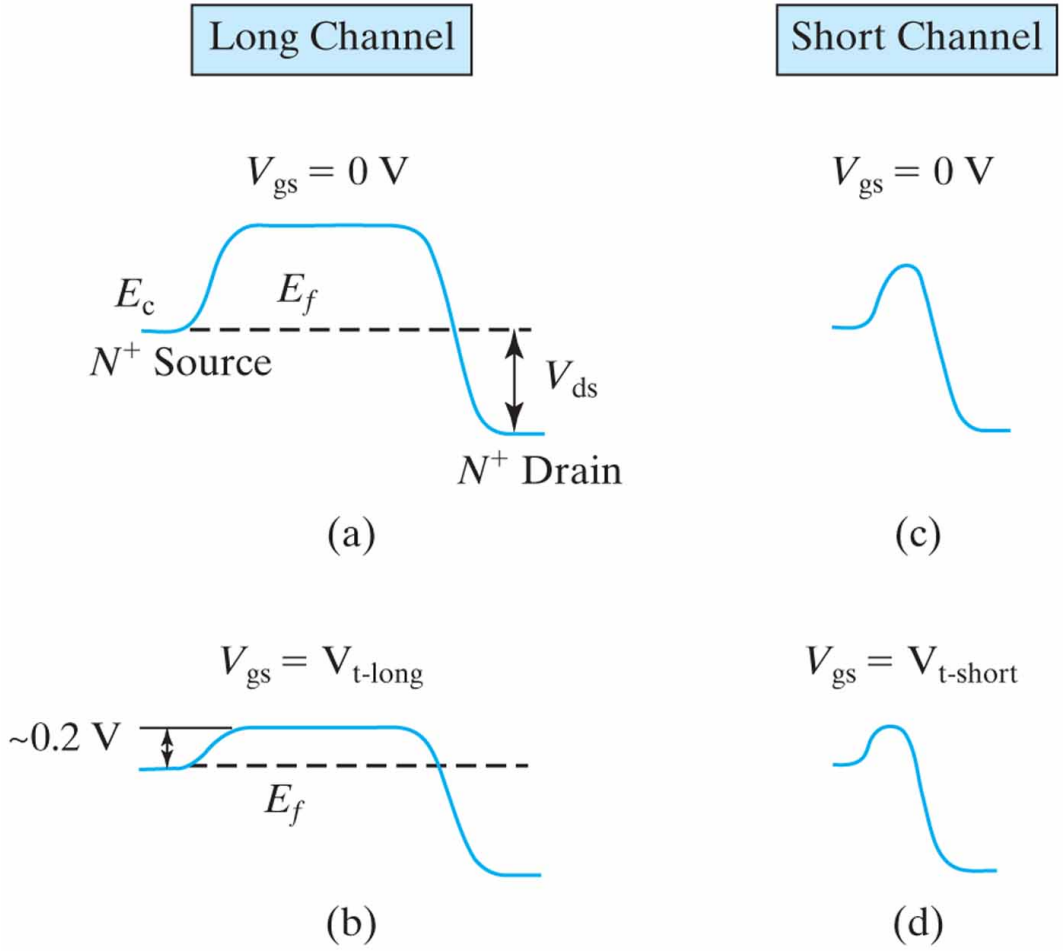

Figure 7.6 Schematic two-capacitor network in MOSFET. C_d models the electrostatic coupling between the channel and the drain. As the channel length is reduced, drain to "channel" distance is reduced; therefore, C_d increases.

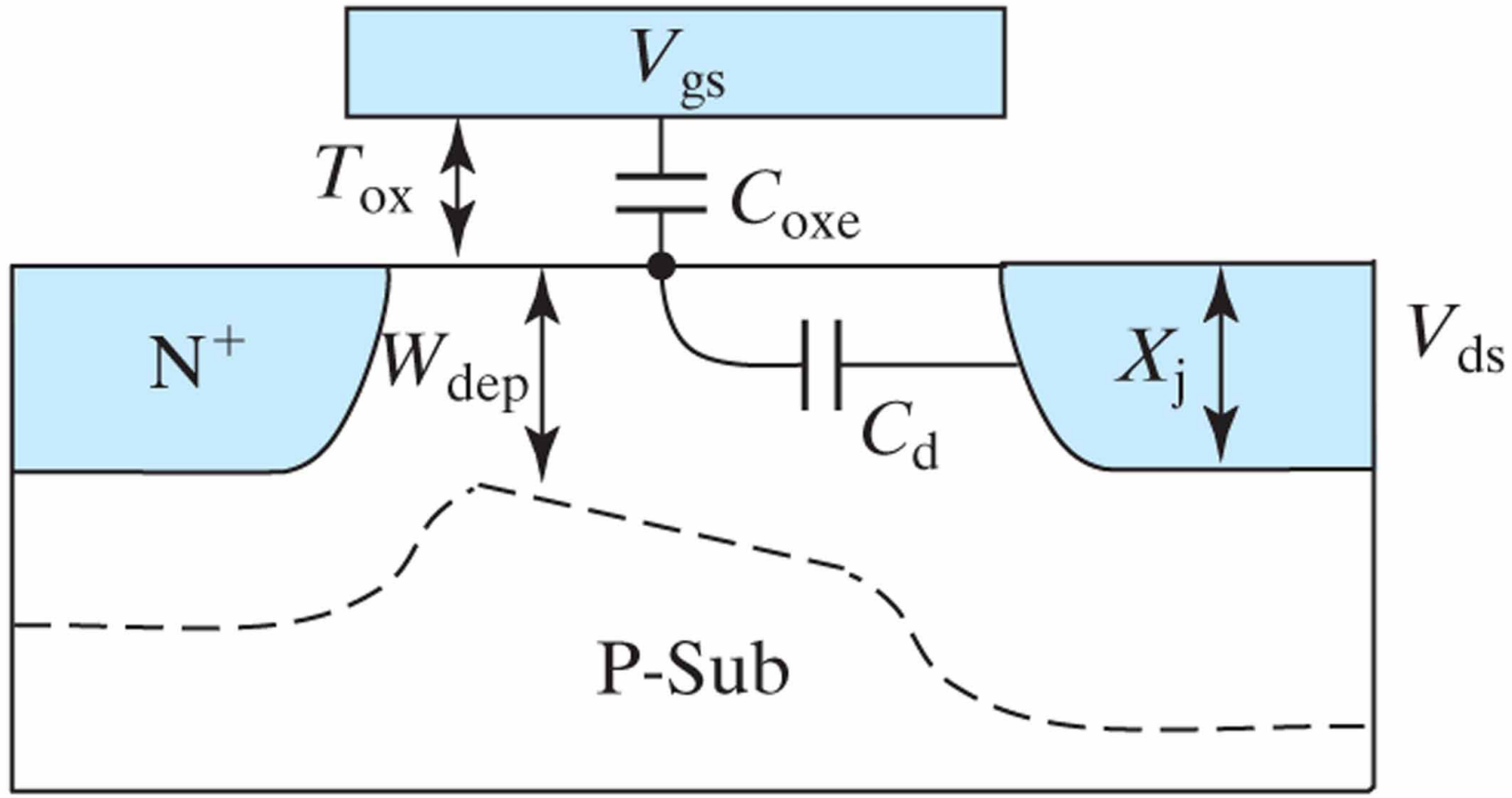

Figure 7.12 Log I_{off} vs. linear I_{on}. The spread in I_{on} (and I_{off}) is due to the presence of several slightly different drawn L_{gs} and unintentional manufacturing variations in L_g and V_t. (After [2]. © 2003 IEEE.)

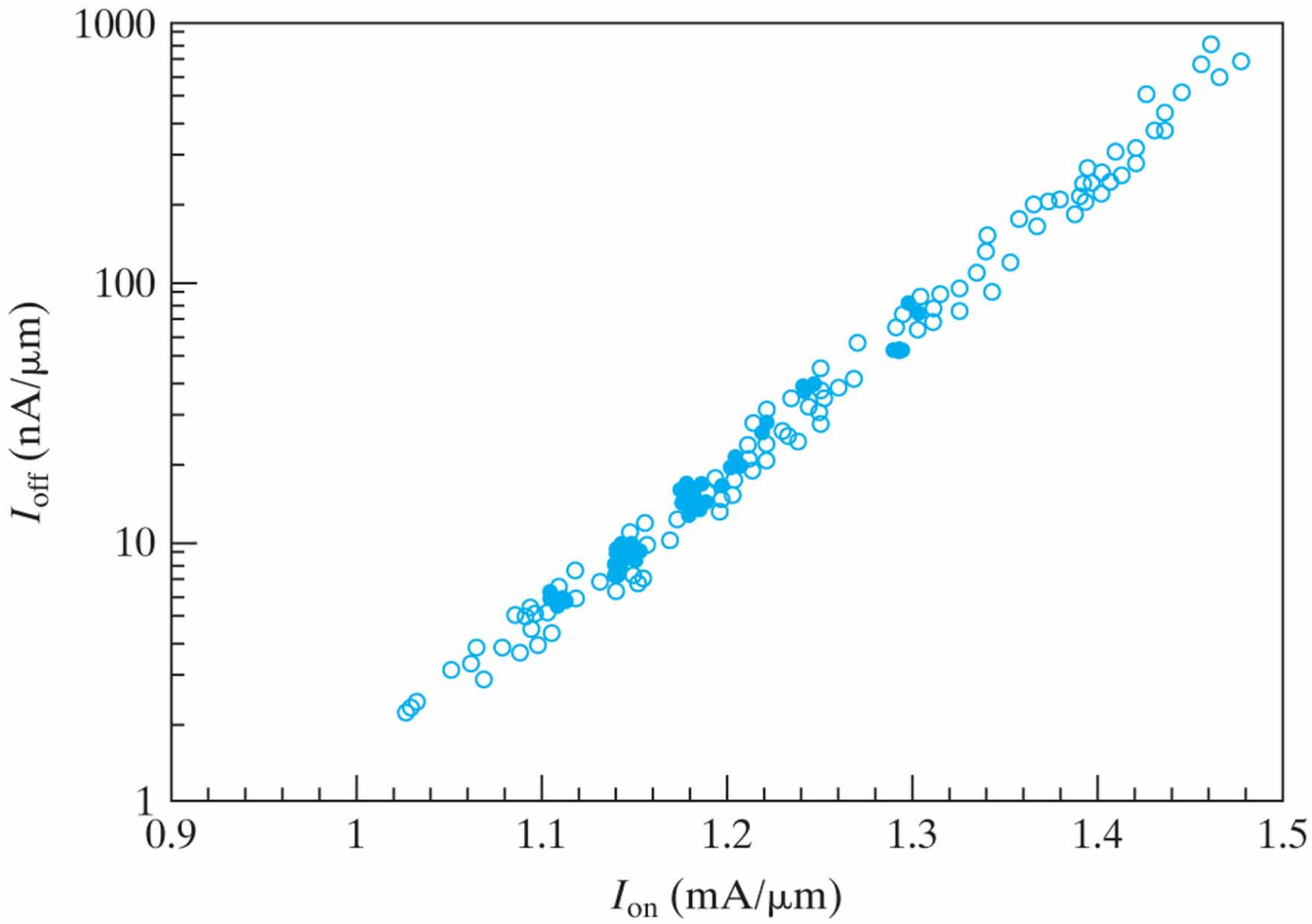

Figure 7.13 The drain could still have more control than the gate along another leakage current path that is some distance below the Si surface.

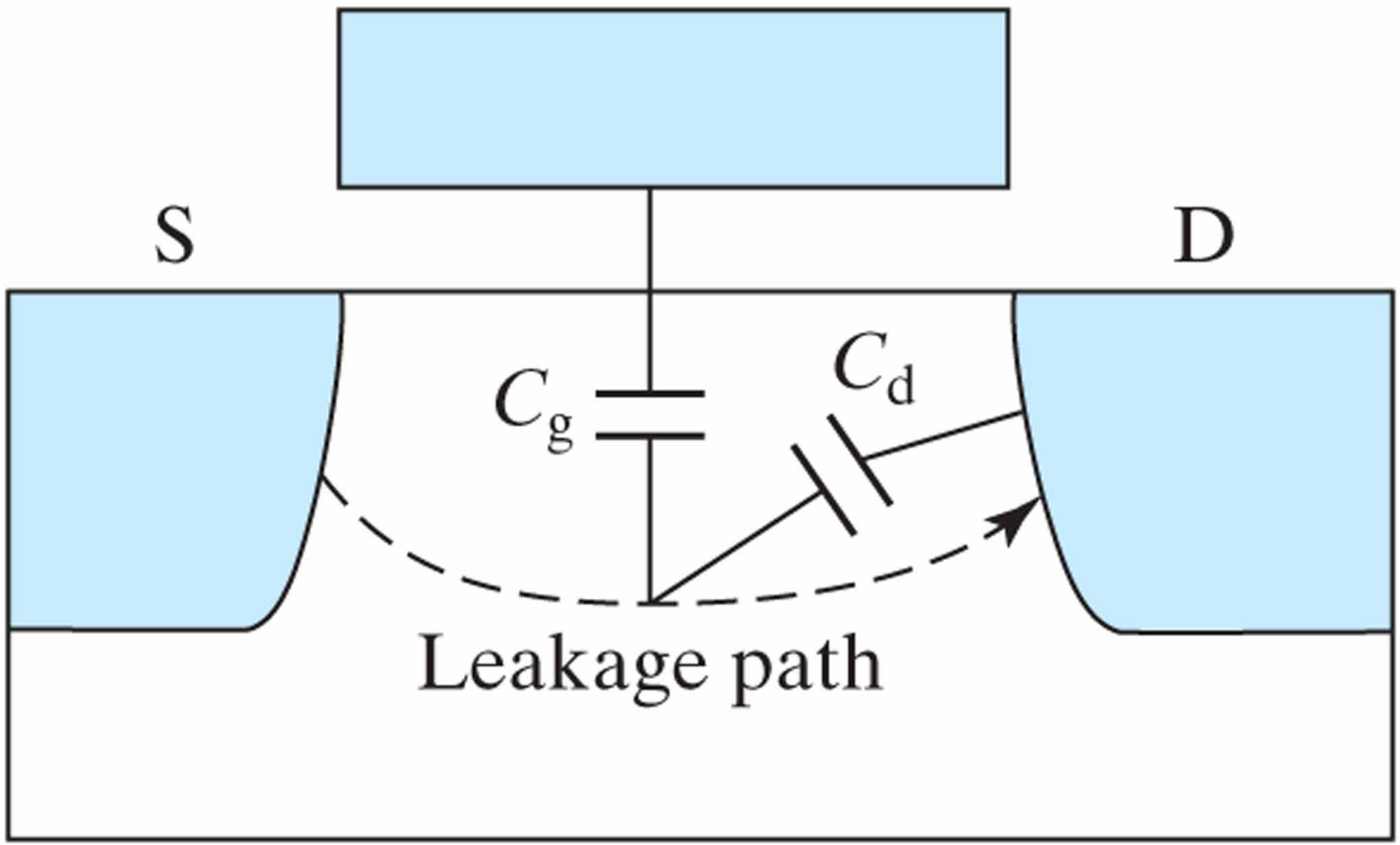

Figure 7.14 The SEM cross section of UTB device. (After [11]. © 2000 IEEE.)

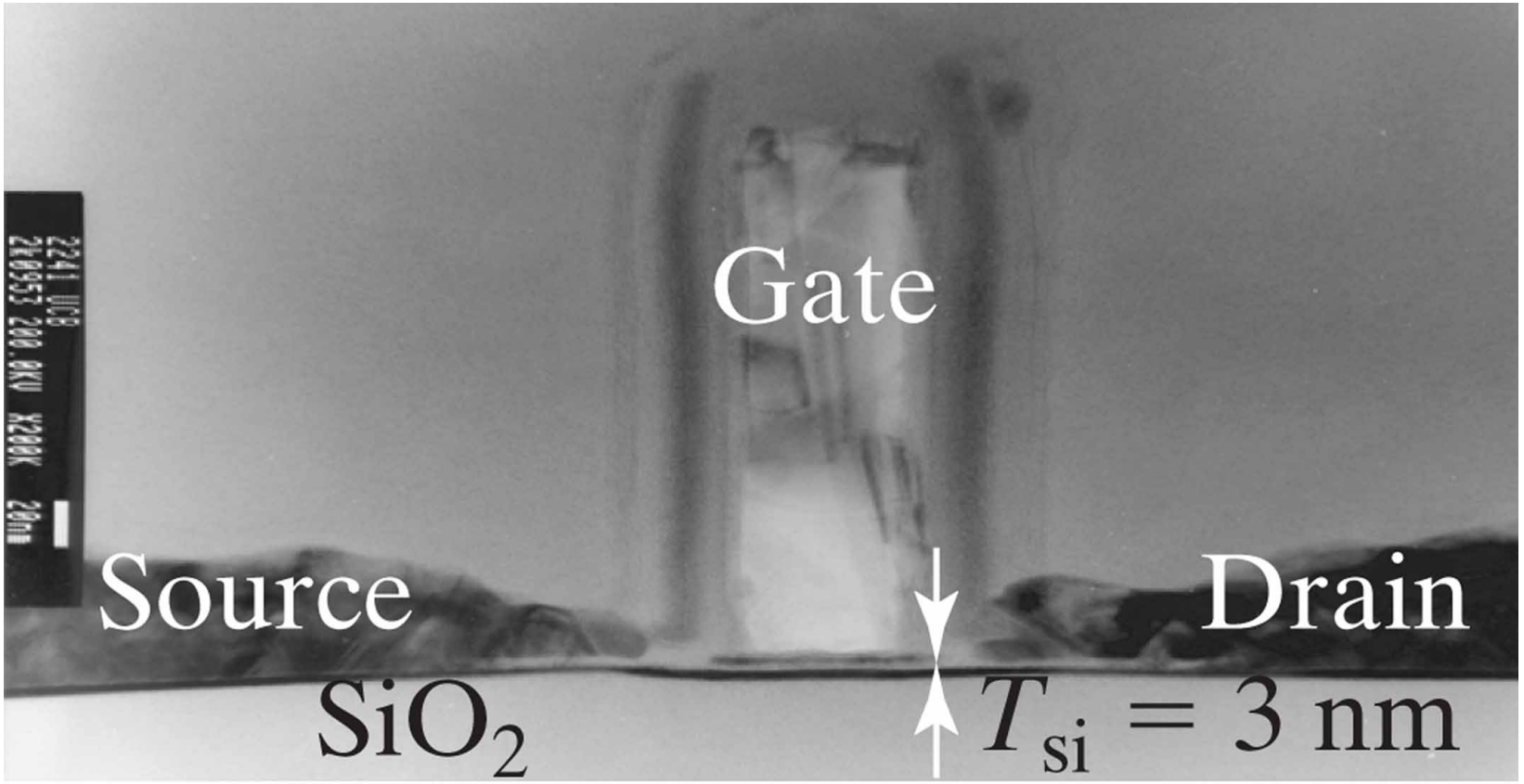

Figure 7.18 A schematic sketch of a double-gate MOSFET with gates connected.

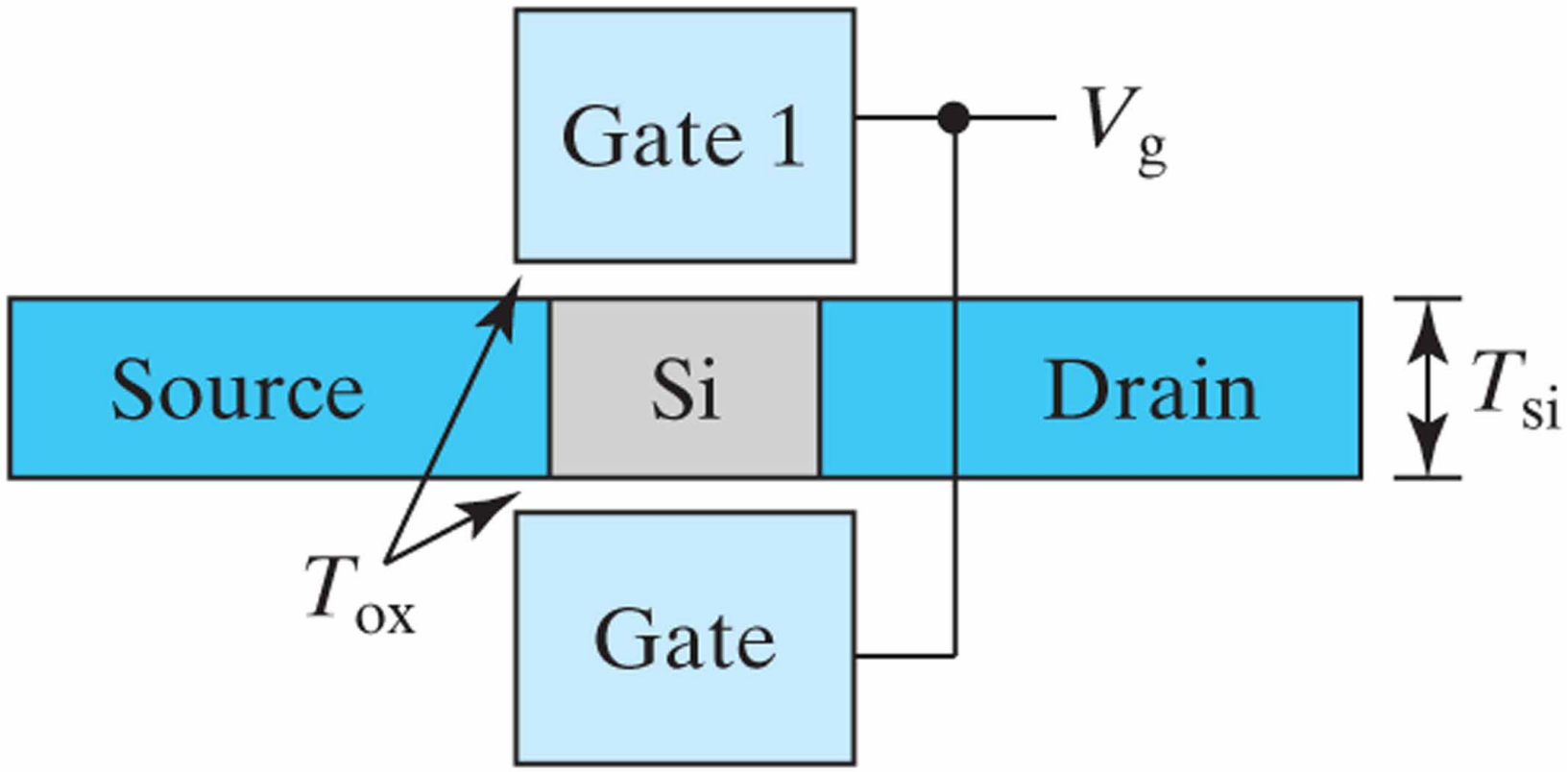

Figure 7.19 Variations of FinFET. Tall FinFET has the advantage of providing a large W and therefore large I_{on} while occupying a small footprint. Short FinFET has the advantage of less challenging lithography and etching. Nanowire FET gives the gate even more control over the transistor body by surrounding it. FinFETs can also be fabricated on bulk Si substrates.