ROYAL INSTITUTE
OF TECHNOLOGY

Semiconductor Devices
Spring 2019

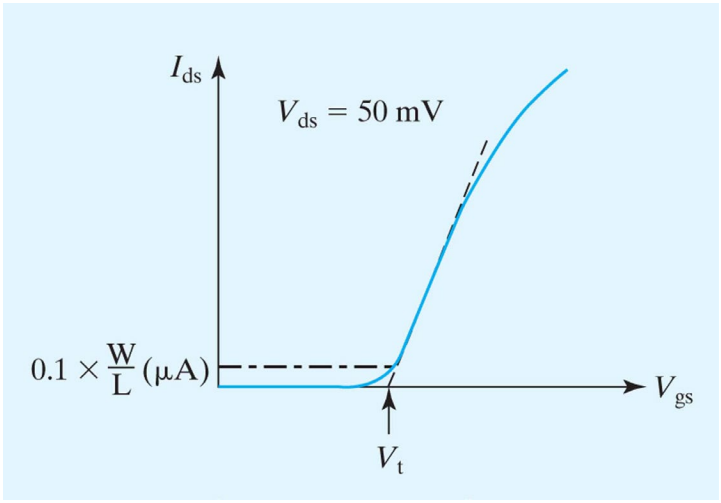
Lecture 9

ROYAL INSTITUTE OF TECHNOLOGY

This Lecture

- Reading
  - Chapter 6, section 7
  - Section 3 (only part related to Fig 6-9)
- Concepts:
  - The CMOS inverter and other basic gates
  - Effective surface mobility in NMOS and PMOS

Figure 6.12 V_t can be measured by extrapolating the I_{ds} vs. V_{gs} curve to $I_{ds} = 0$. Alternatively, it can be defined as the V_{gs}, at which I_{ds} is a small fixed amount.



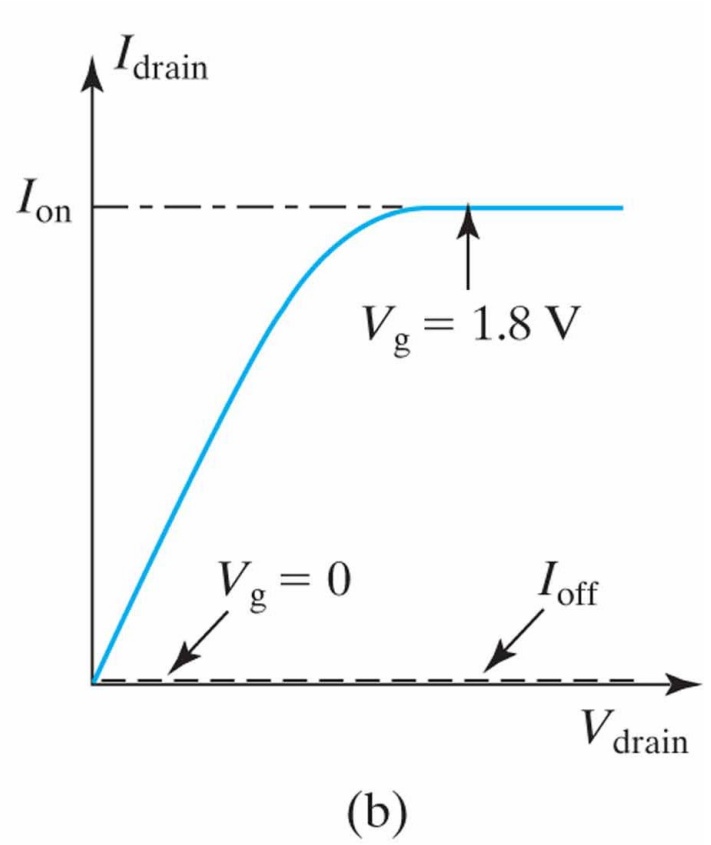


Figure 6.17 (a)−(d) $V_{ds} = V_{dsat}$ and (e)−(h) $V_{ds} > V_{dsat}$. Current does not change when V_{ds} increases beyond V_{dsat}. (d) and (h) are $E_c(x)$ from the energy band diagrams.

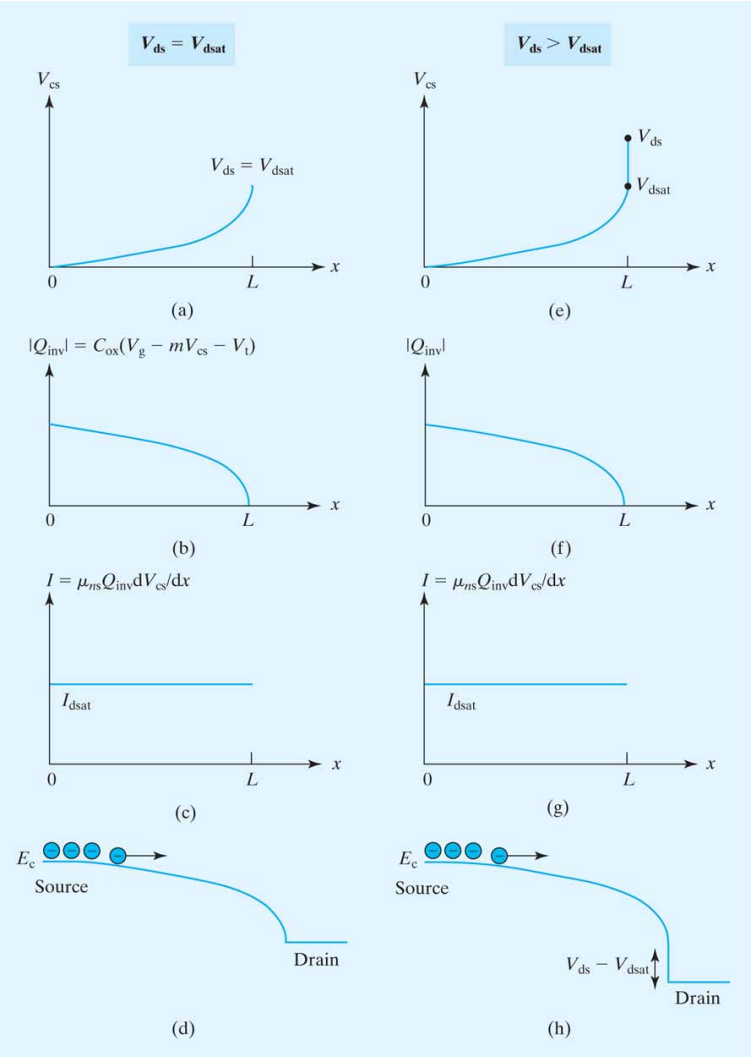


Figure 6.39

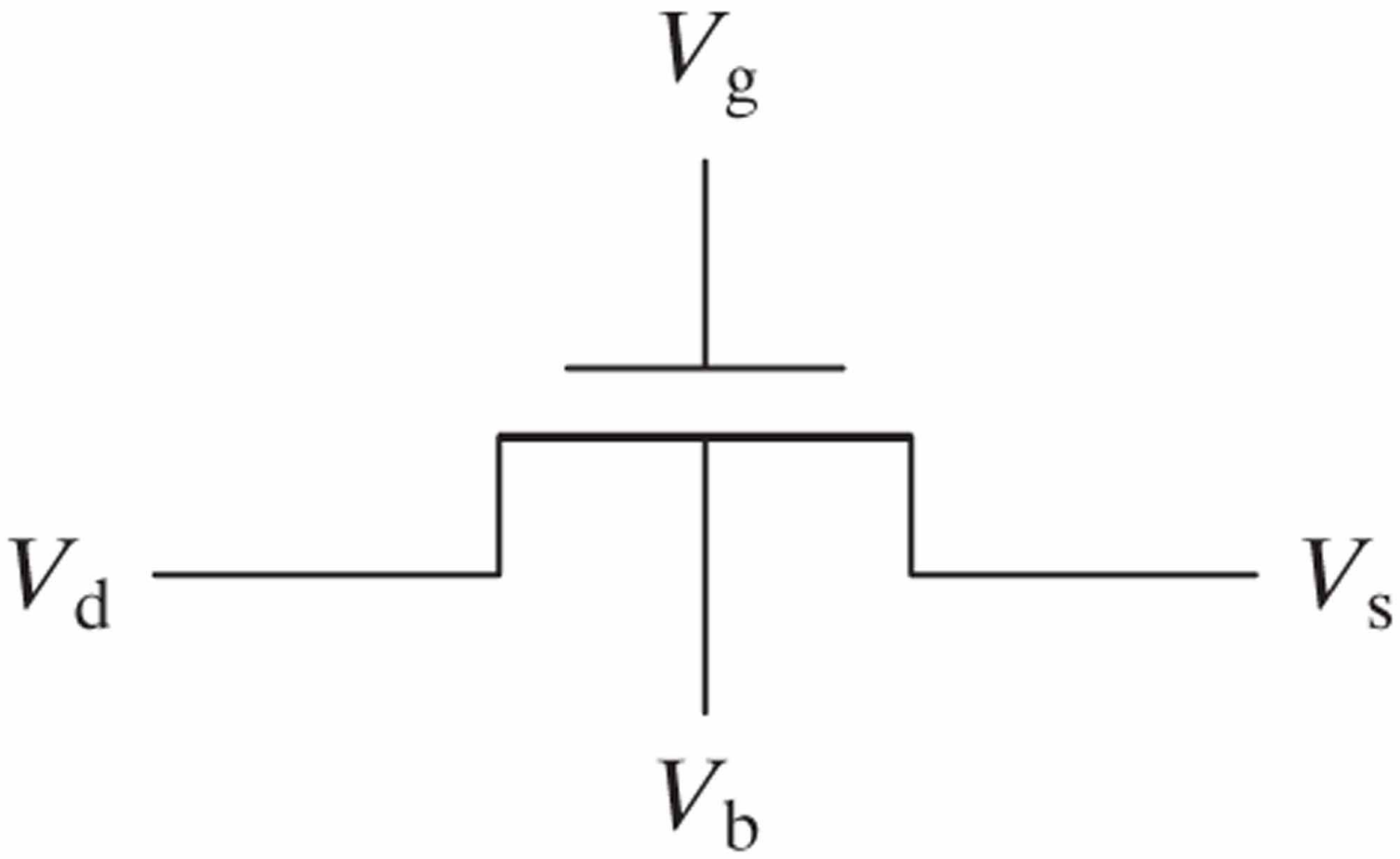
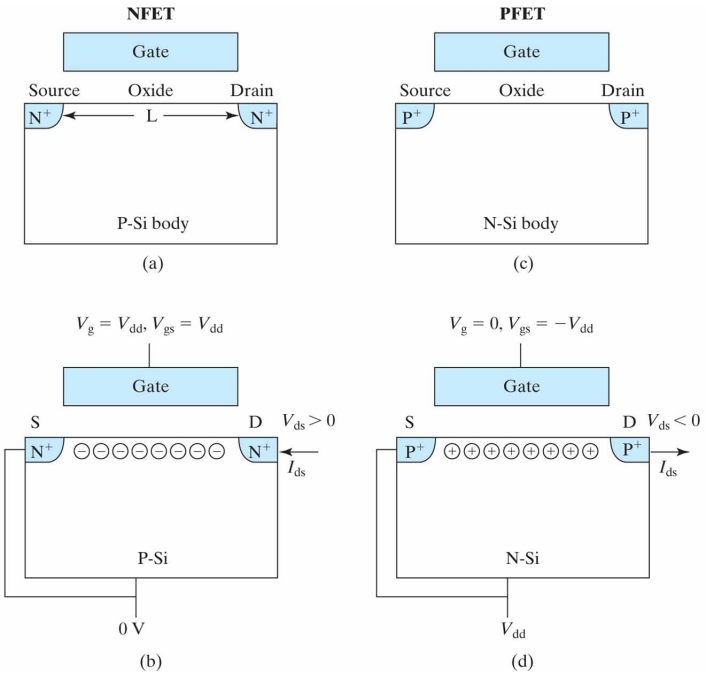
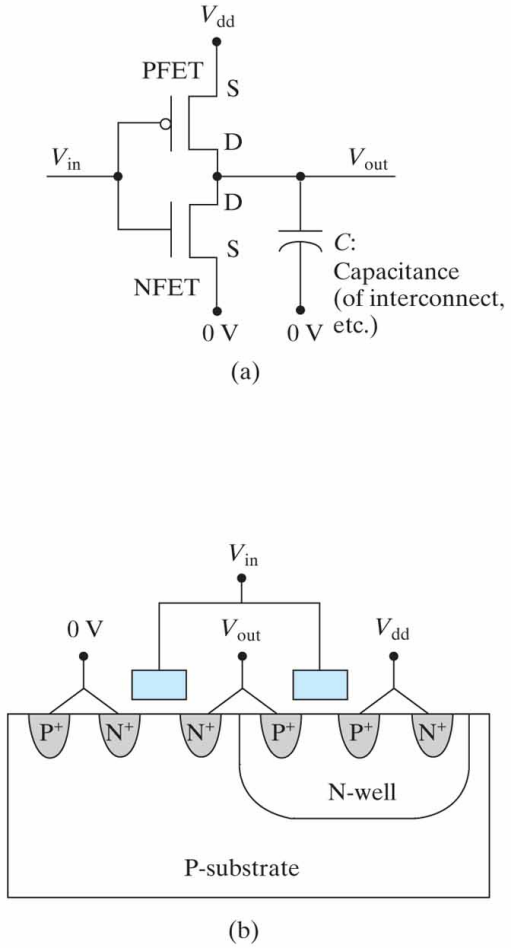


Figure 6.7 Three views of a CMOS inverter. (a) A CMOS inverter consists of a PFET **pull-up device** and an NFET **pull-down device**. (b) Integration of NFET and PFET on the same chip. For simplicity, trench isolation (see Fig. 6–1), which fills all the surface area except for the diffusion regions and the channel regions, is not shown. (c) Layout of a CMOS inverter.





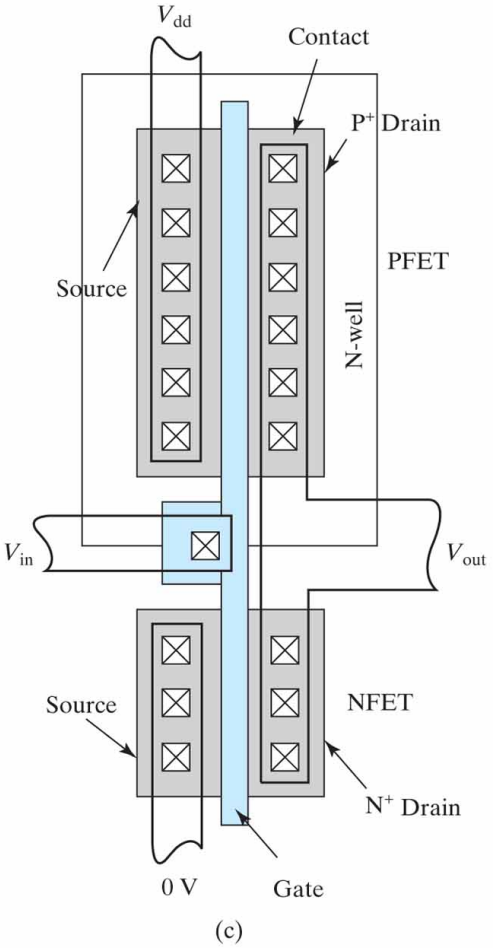


Figure 6.8 Surface mobility is a function of the average of the electric fields at the bottom and the top of the inversion charge layer, $\mathscr{E}_b$ and $\mathscr{E}_t$.

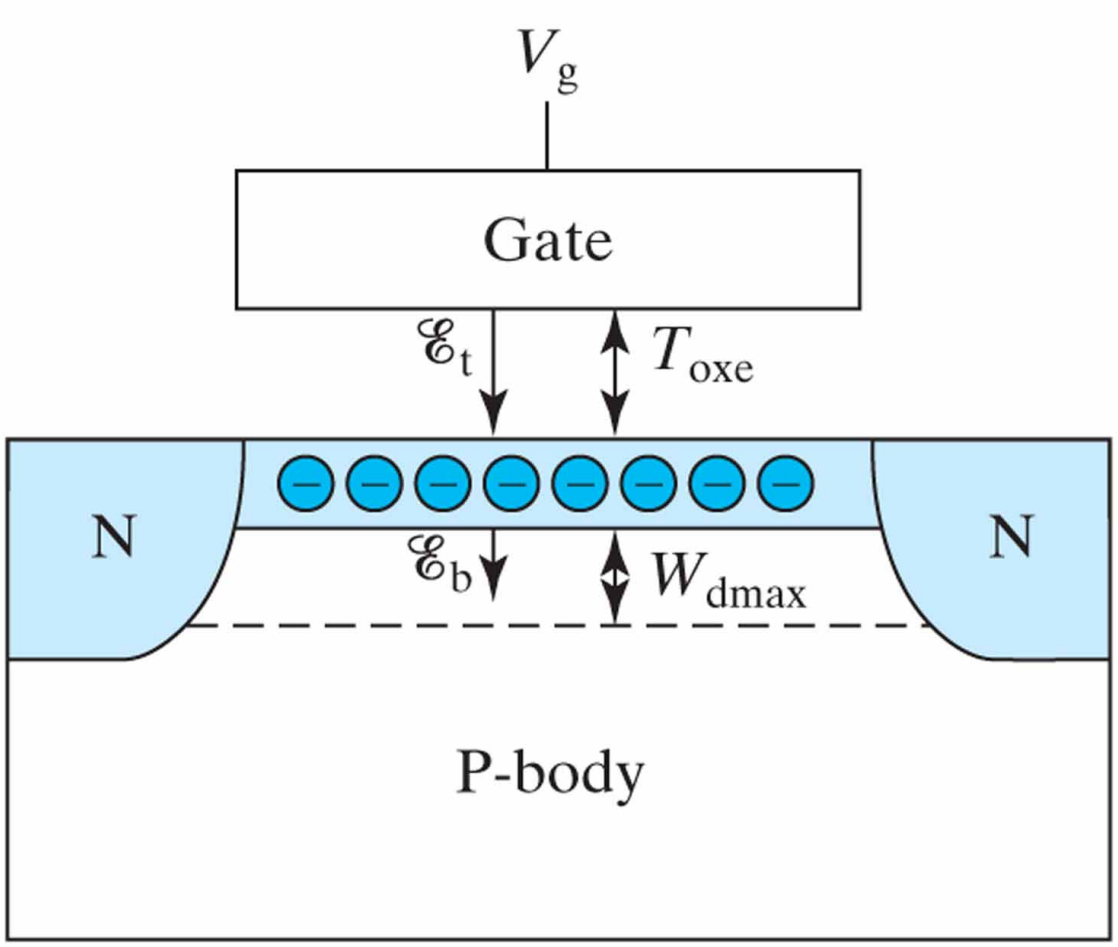


Figure 6.9 Electron and hole surface mobilities are determined by V_{gs}, V_t, and T_{oxe}. T_{oxe} is the SiO_2 equivalent electrical oxide thickness. (From [4]. © 1996 IEEE.)

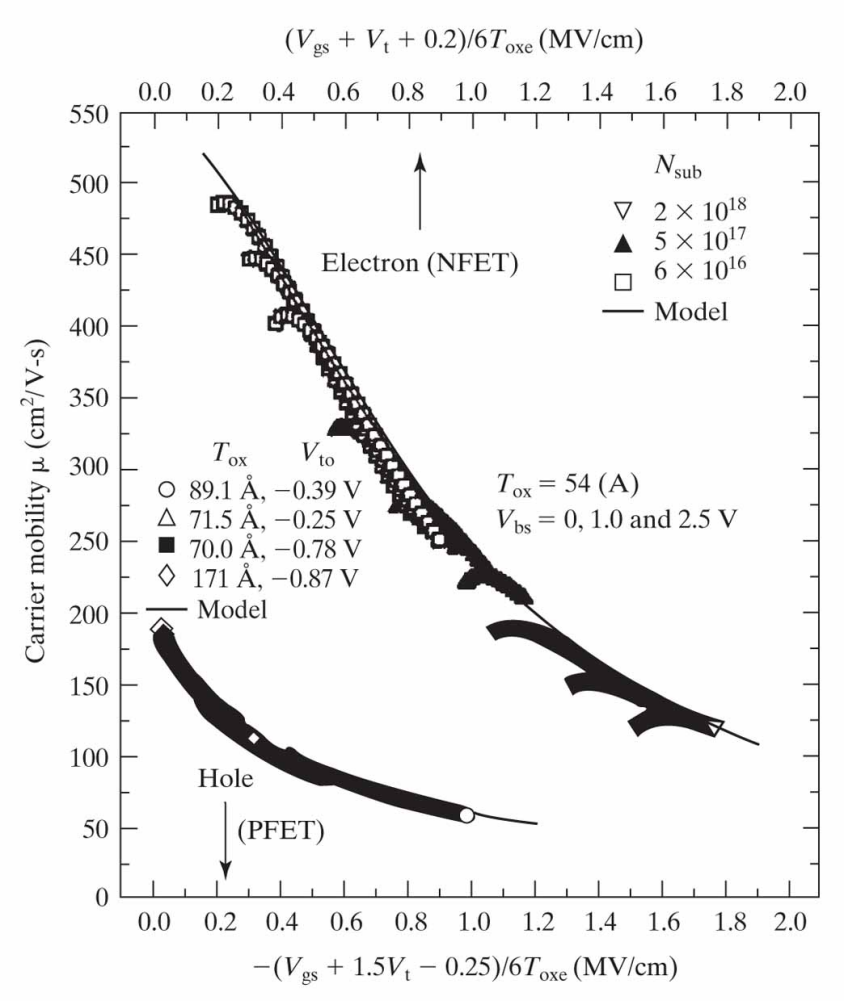


Figure 6.23 Measured IV characteristics. (a) A 0.15 μm channel device (V_t = 0.4 V) shows a linear relationship between I_{dsat} and V_{gs}. V_{dsat} is significantly less than $V_{gs} - V_t$. (b) A 2 μm device (Vt = 0.7 V) exhibits the $I_{dsat} \propto (V_{gs} - V_t)^2$ relationship. (c) IV characteristics of PFET and NFET with T_{oxe} = 3 nm and $L \approx$ 100 nm.

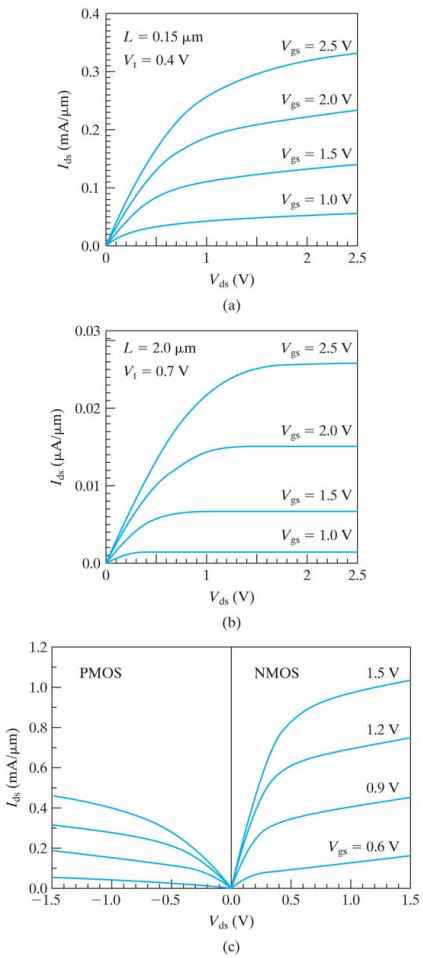


Figure 6.29 A simple MOSFET amplifier.

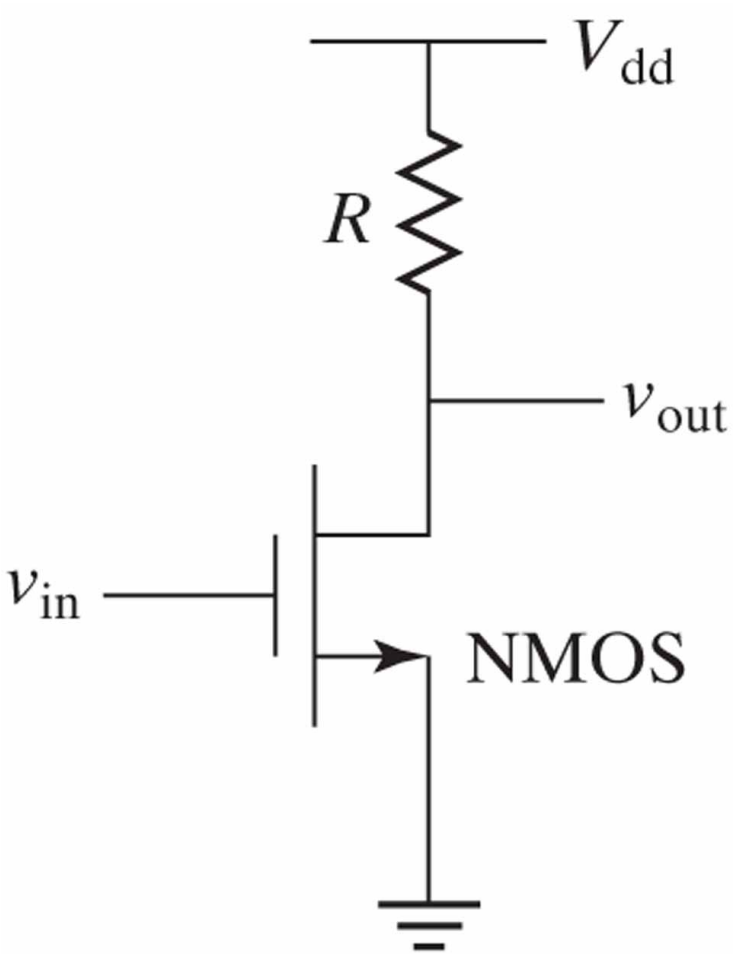


Figure 6.18 (a) CMOS inverter; (b) IV characteristics of NFET and PFET; and (c) $V_{out} = V_{dsN} = 2\text{ V} + V_{dsP}$ according to (a).

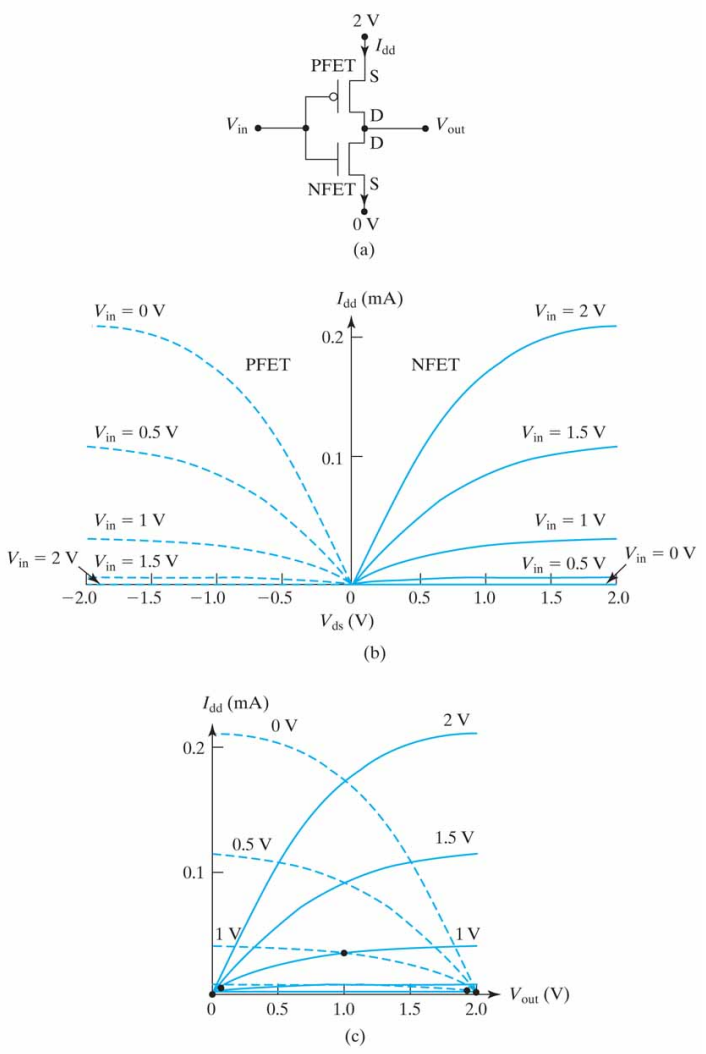


Figure 6.19 The VTC of a CMOS inverter.

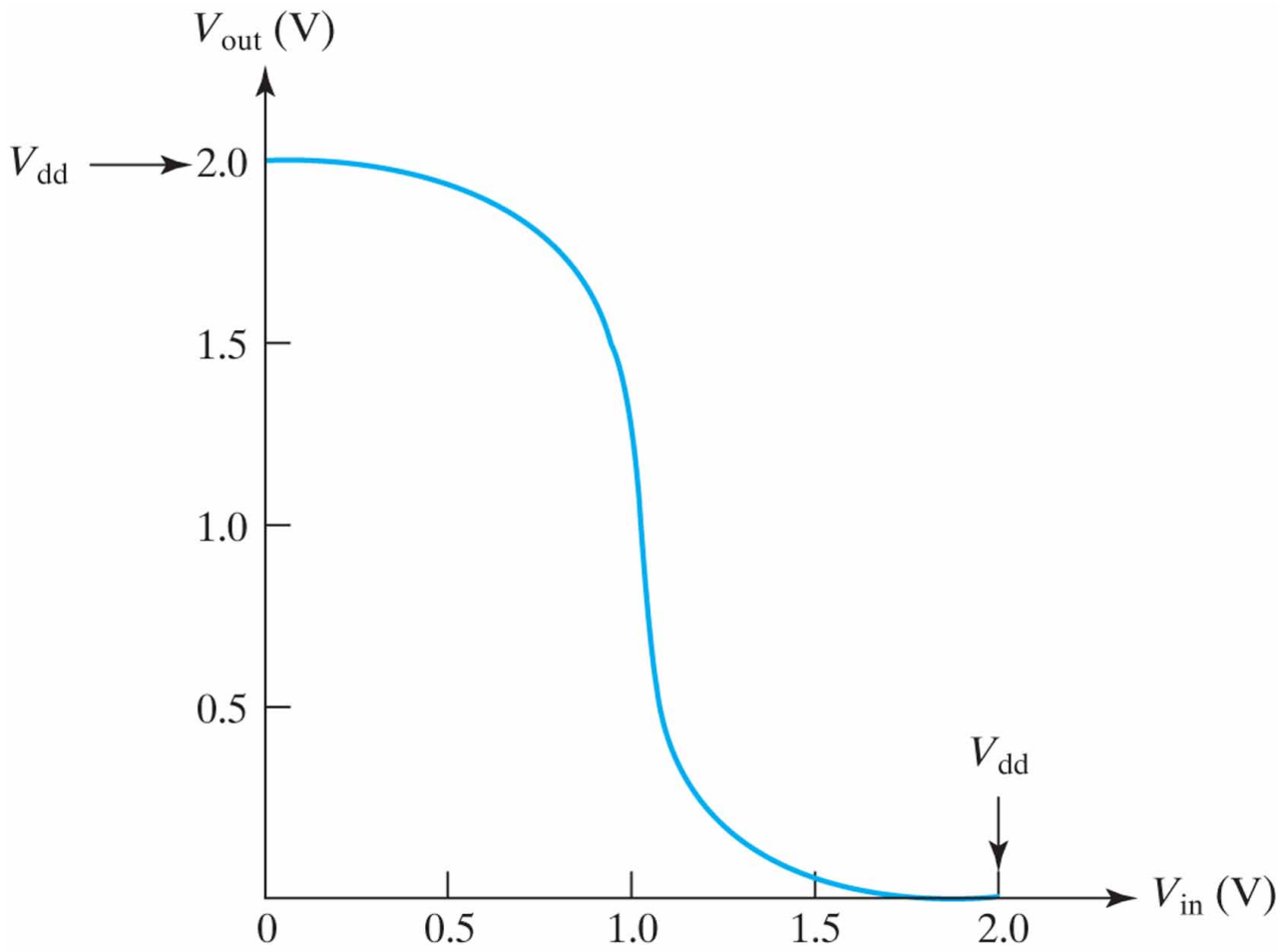


Figure 6.20 (a) A CMOS inverter chain. A circle on the gate indicates a PFET. (b) Propagation delay, $\mathscr{T}_d$, defined.

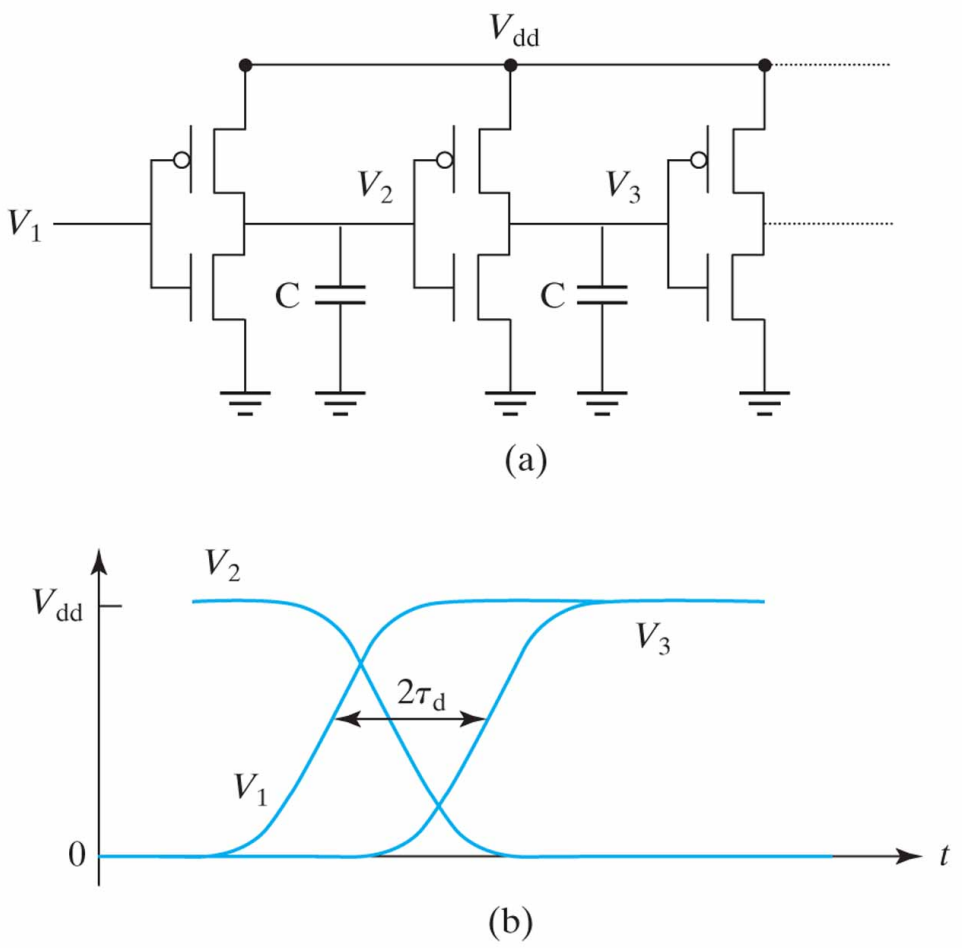


Figure 6.21 Inverters are the foundation of more complex circuits such as this two-input NAND gate.

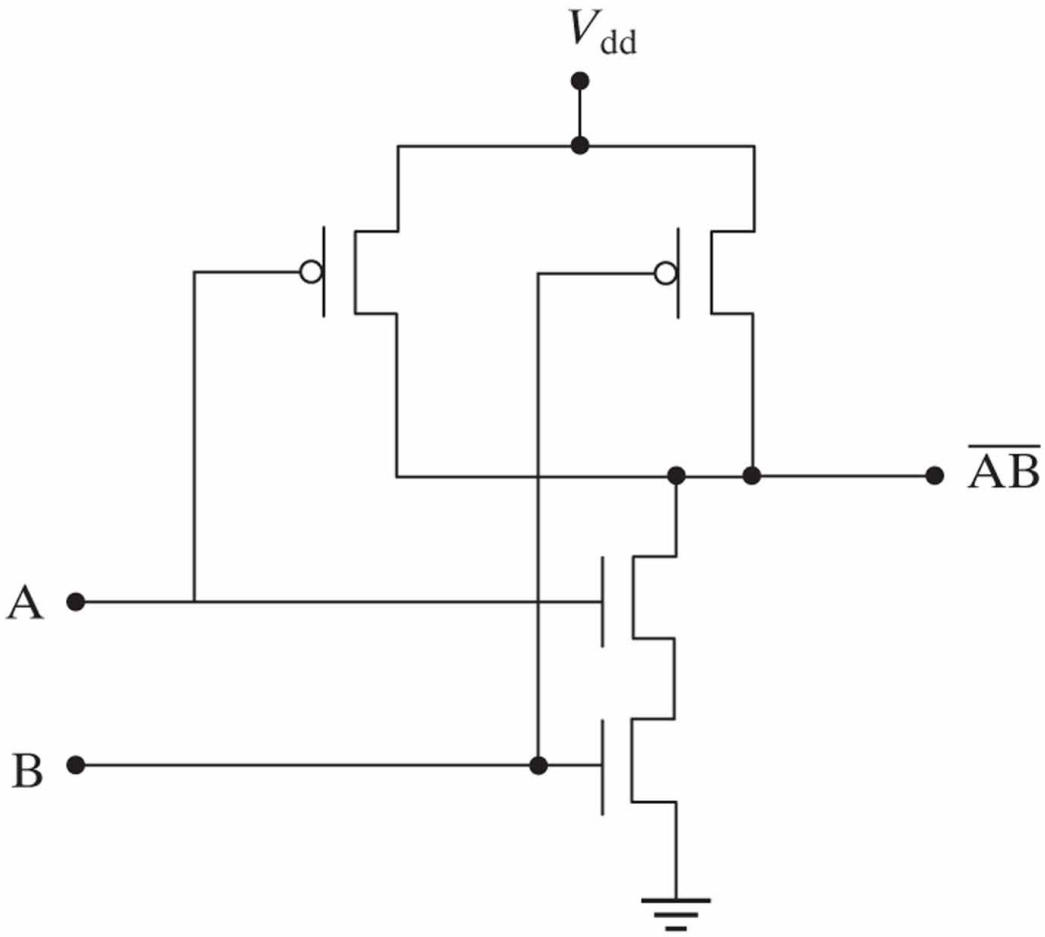


Figure 6.46