ROYAL INSTITUTE
OF TECHNOLOGY

Semiconductor Devices
Spring 2019

Lecture 8

ROYAL INSTITUTE OF TECHNOLOGY

This Lecture

- Reading
  - Chapter 5, sections 1-6
- Concepts:
  - Metal-oxide-semiconductor (MOS)
  - The FIELD effect transistor (focus on p-channel)

Figure 5.2 An MOS transistor is an MOS capacitor with PN junctions at two ends.

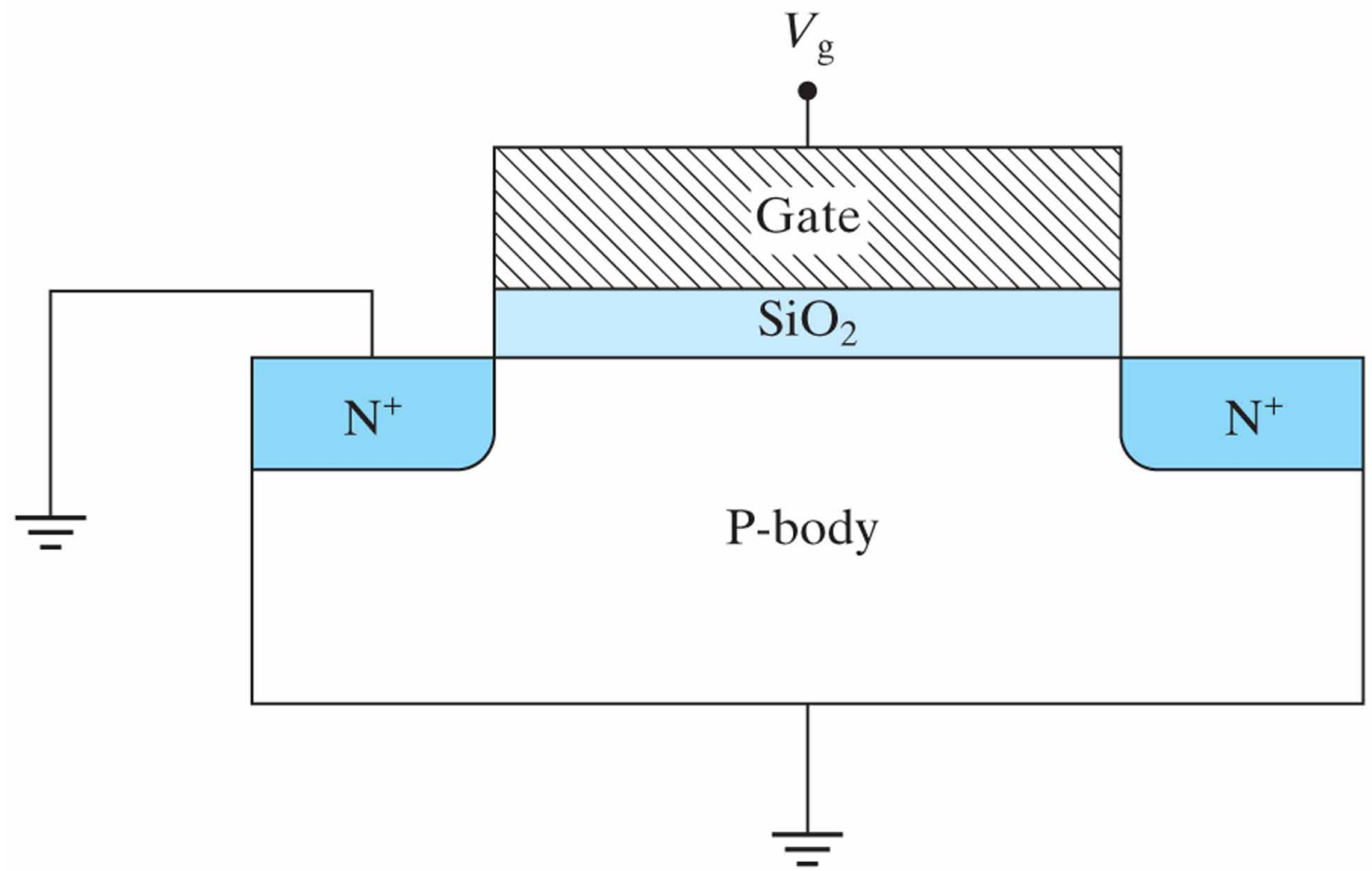

Figure 6.1 (a) Basic MOSFET structure and (b) IV characteristics.

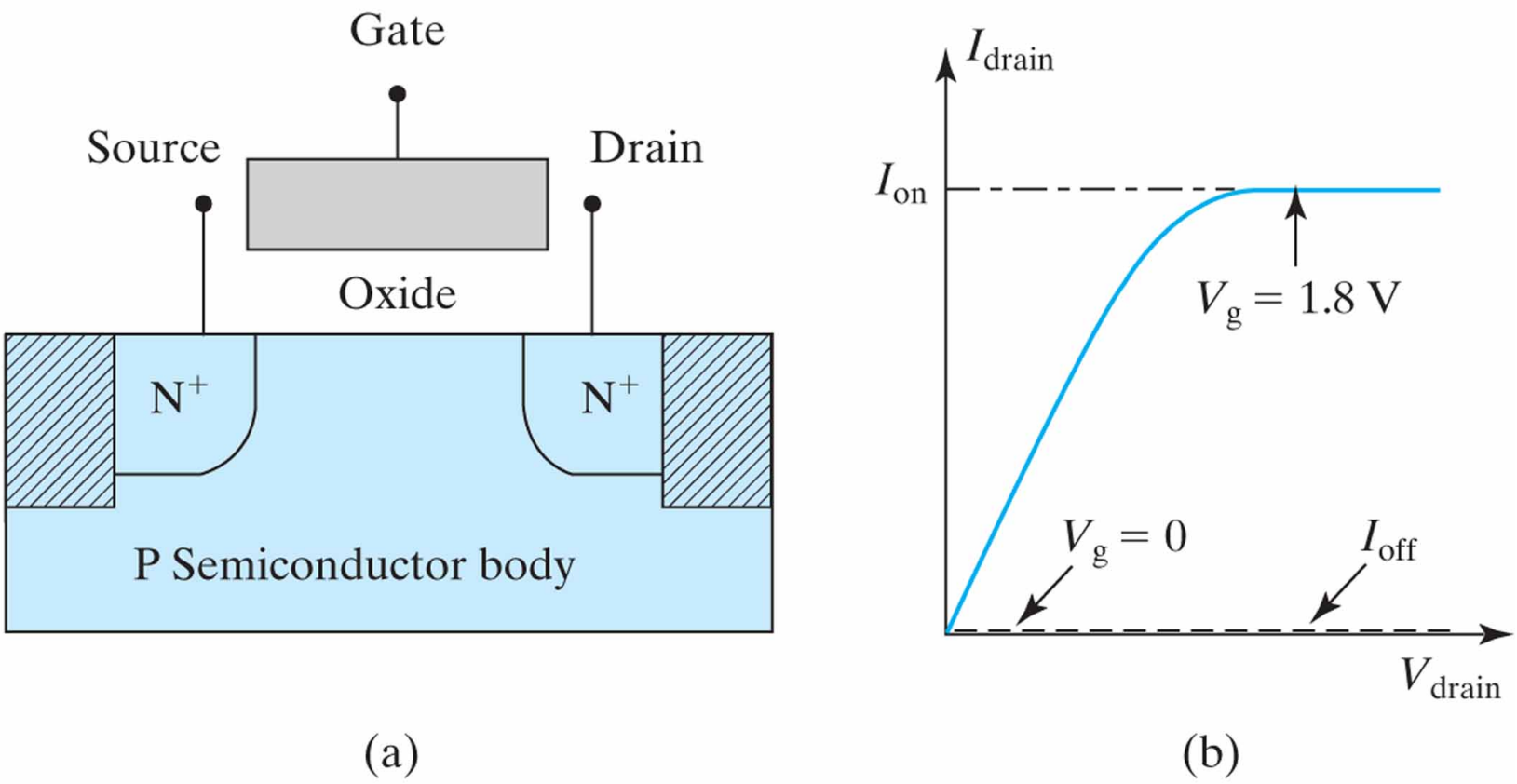

Figure 6.2 Two ways of representing a MOSFET: (a) a circuit symbol and (b) as an on/offswitch.

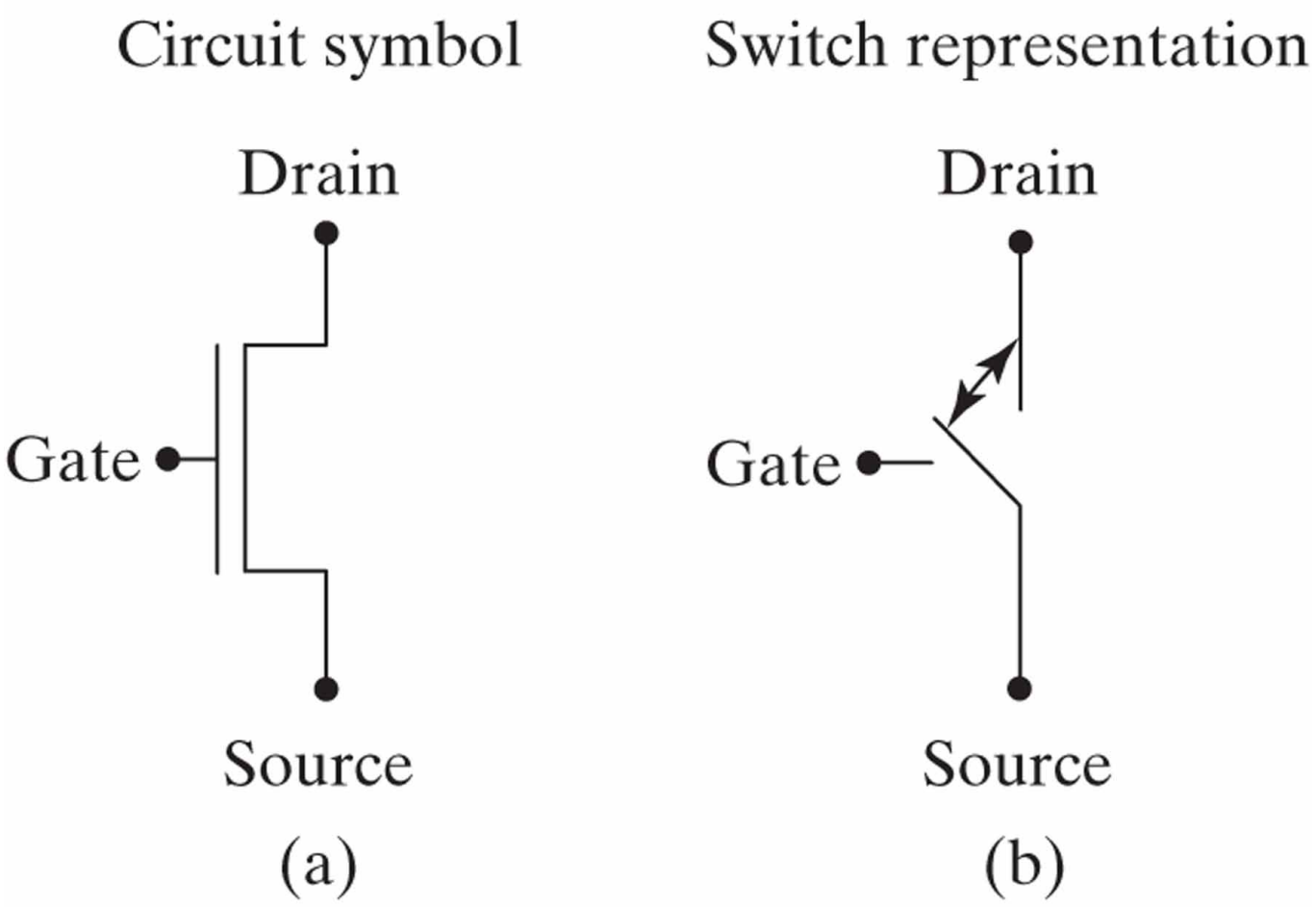

Figure 5.1 The MOS capacitor.

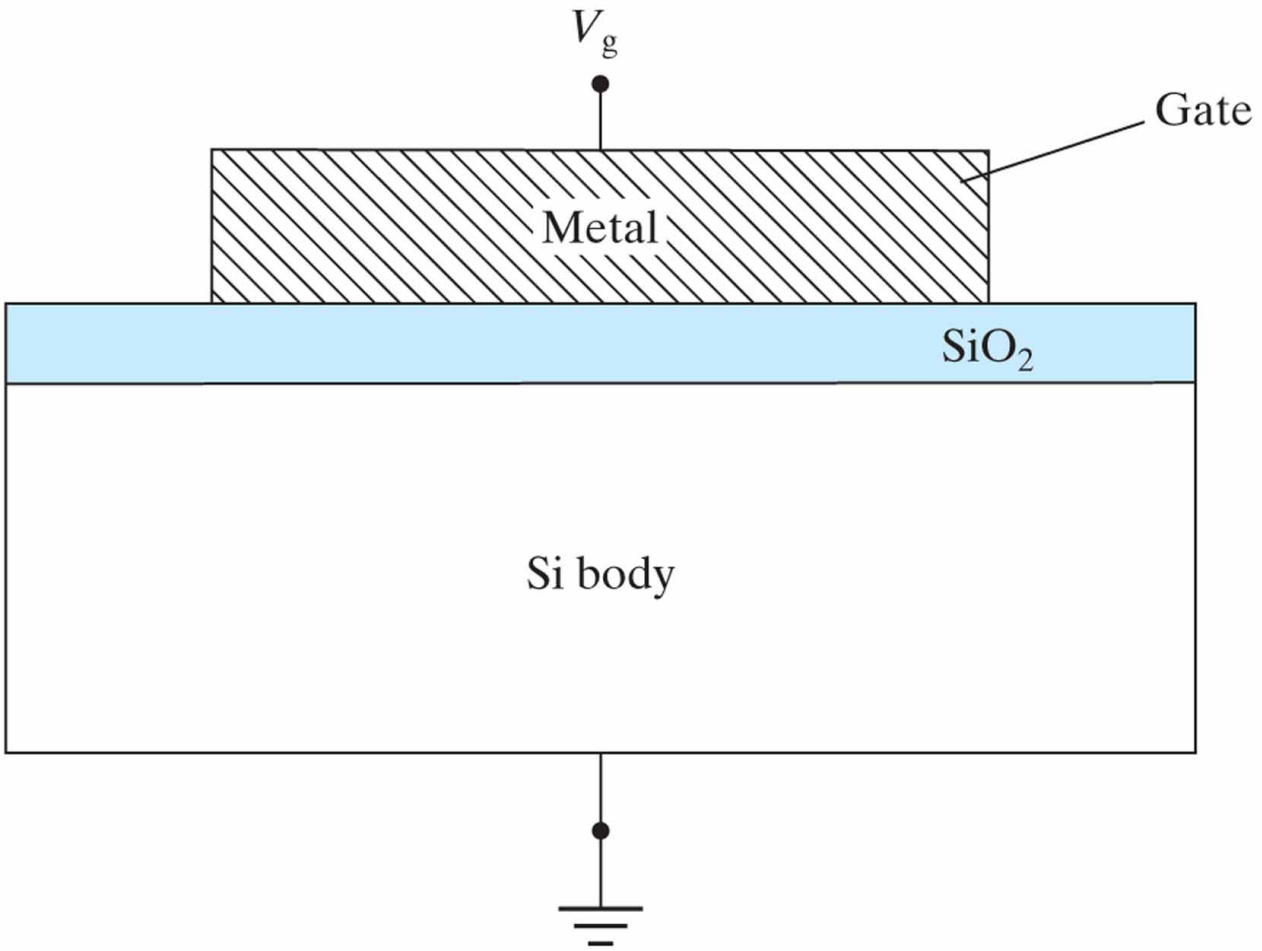

Figure 5.3 (a) Polysilicon-gate/oxide/semiconductor capacitor and (b) its energy band diagram with no applied voltage.

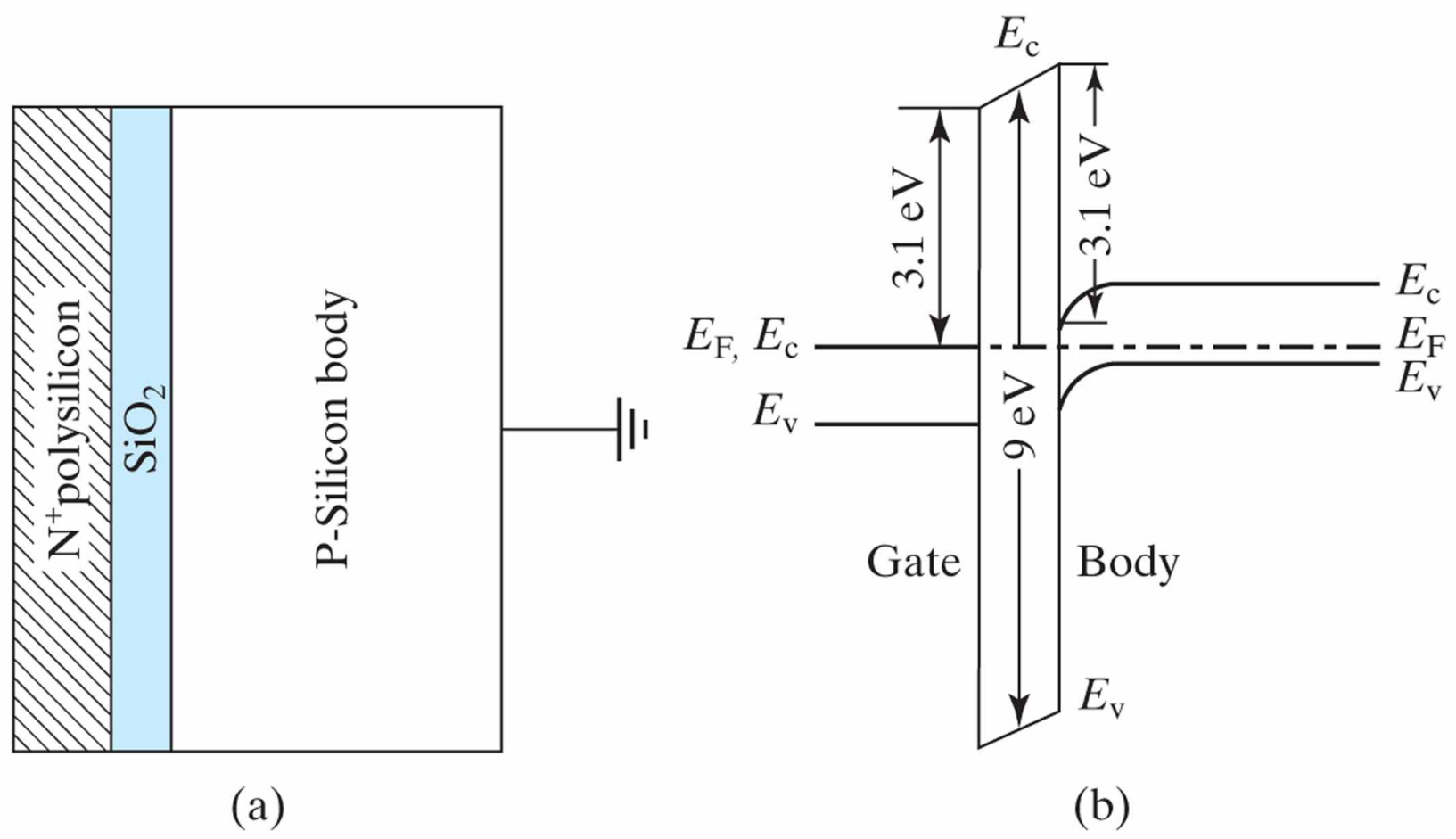

Figure 5.4 Energy band diagram of the MOS system at the flat-band condition. A voltage equal to V_{fb} is applied between the N^+-poly-Si gate and the P-silicon body to achieve this condition. ψ_g is the gate-material work function, and ψ_s is the semiconductor work function. E_0 is the vacuum level.

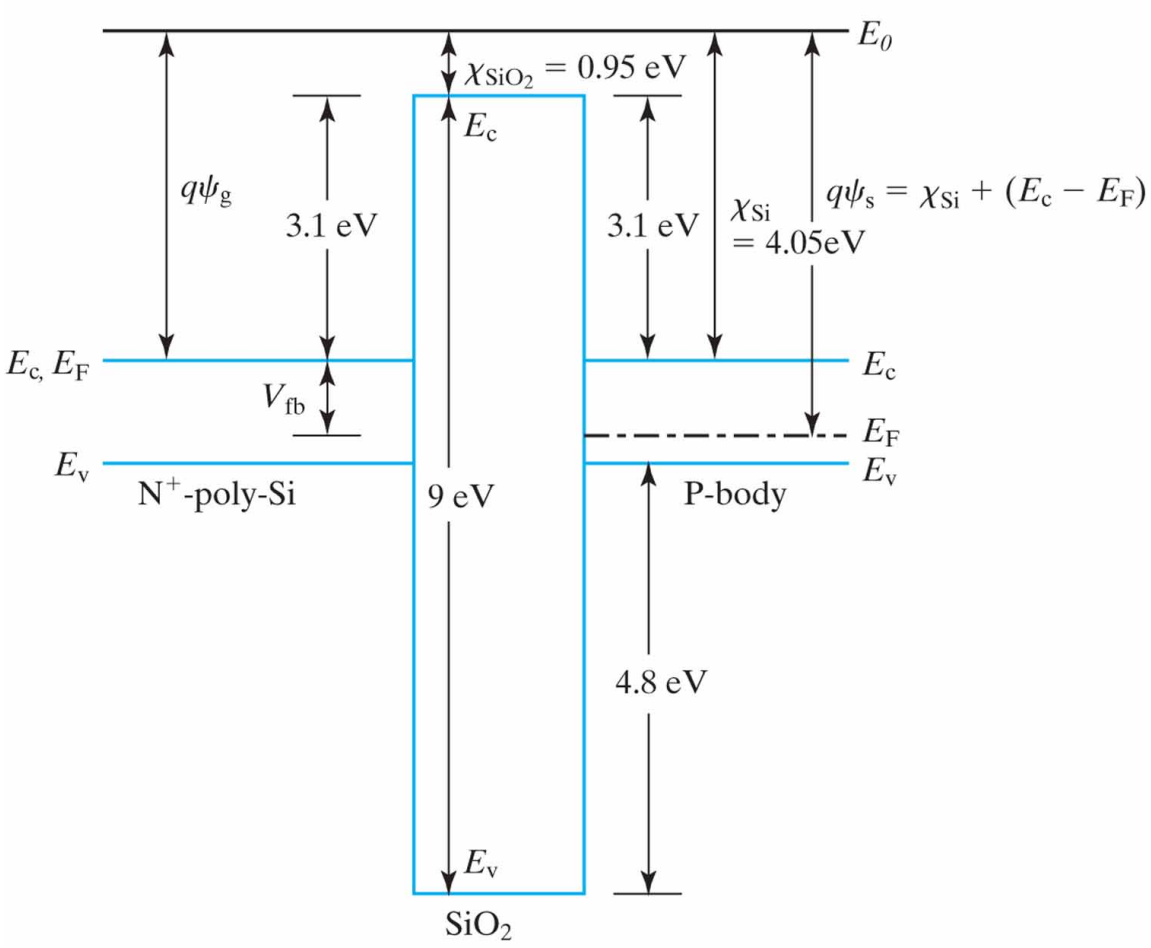

Figure 5.5 This MOS capacitor is biased into surface accumulation ($p_s > p_0 = N_a$). (a) Types of charge present. ⊕ represents holes and – represents negative charge. (b) Energy band diagram.

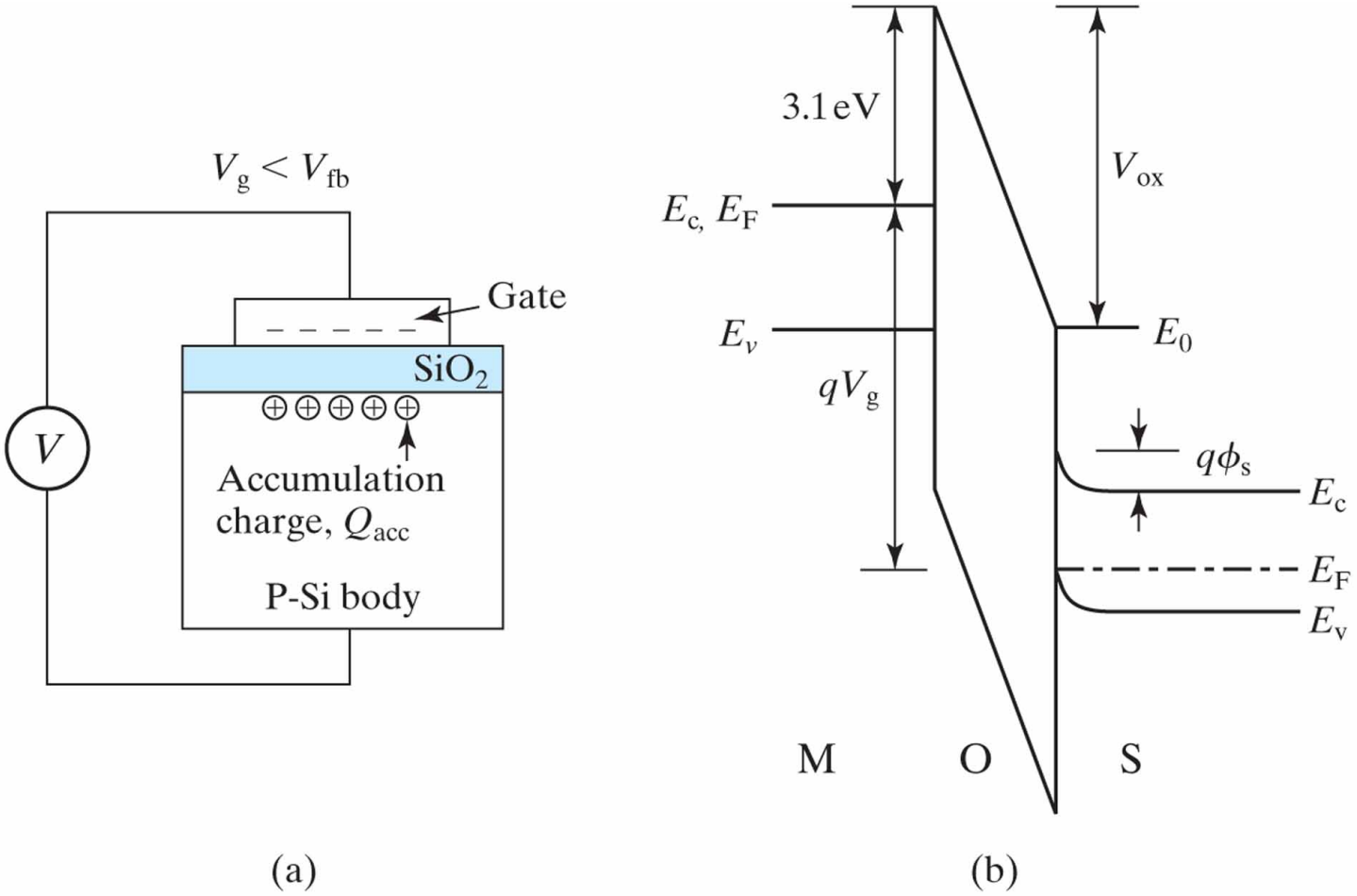

Figure 5.6 This MOS capacitor is biased into surface depletion. (a) Types of charge present; (b) energy band diagram.

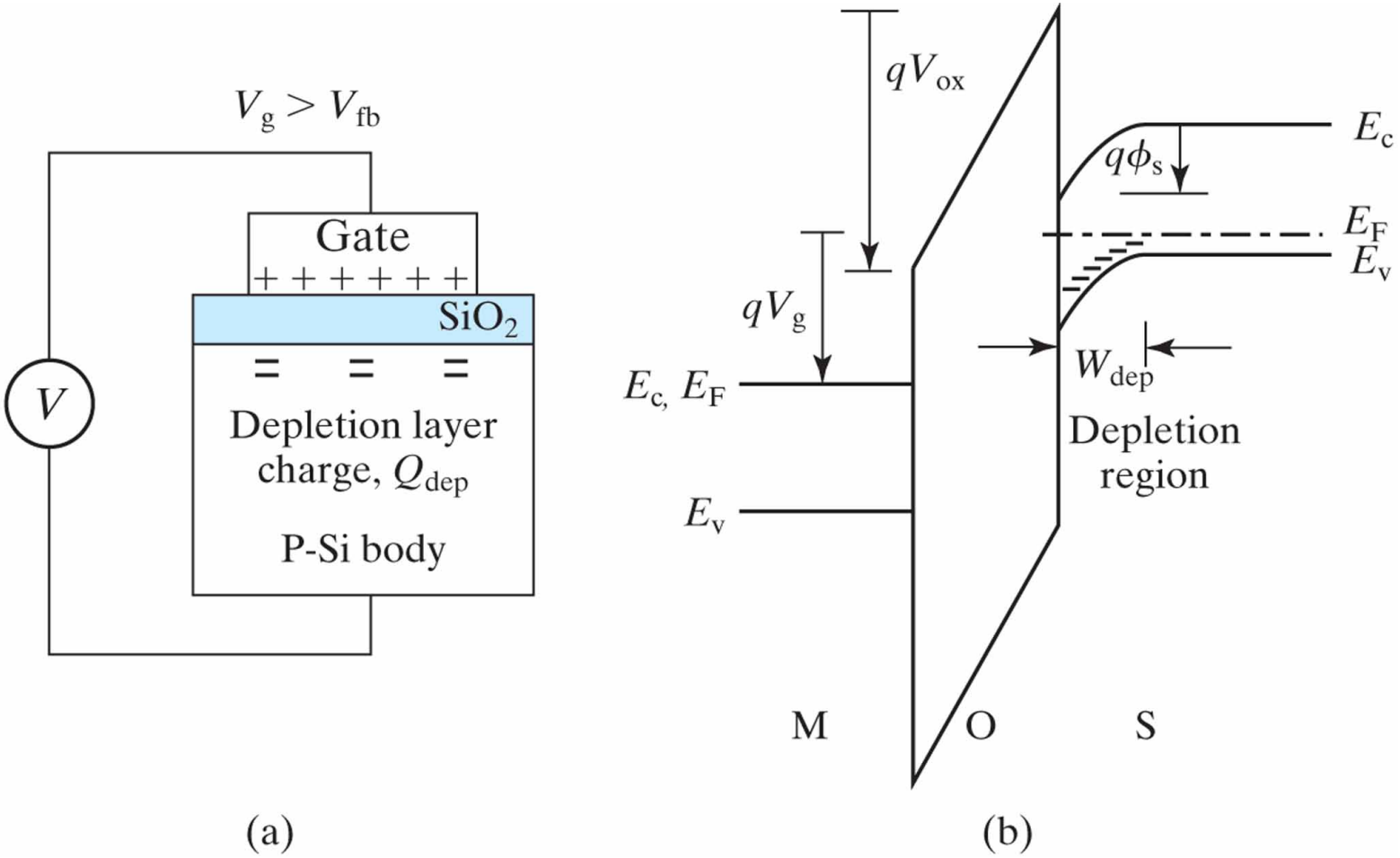

Figure 5.7 The threshold condition is reached when $n_s = N_a$, or equivalently, $A = B$, or $\phi_s = \phi_{st} = 2\,\phi_B$. Note that positive ϕ_{st} corresponds to downward band bending.

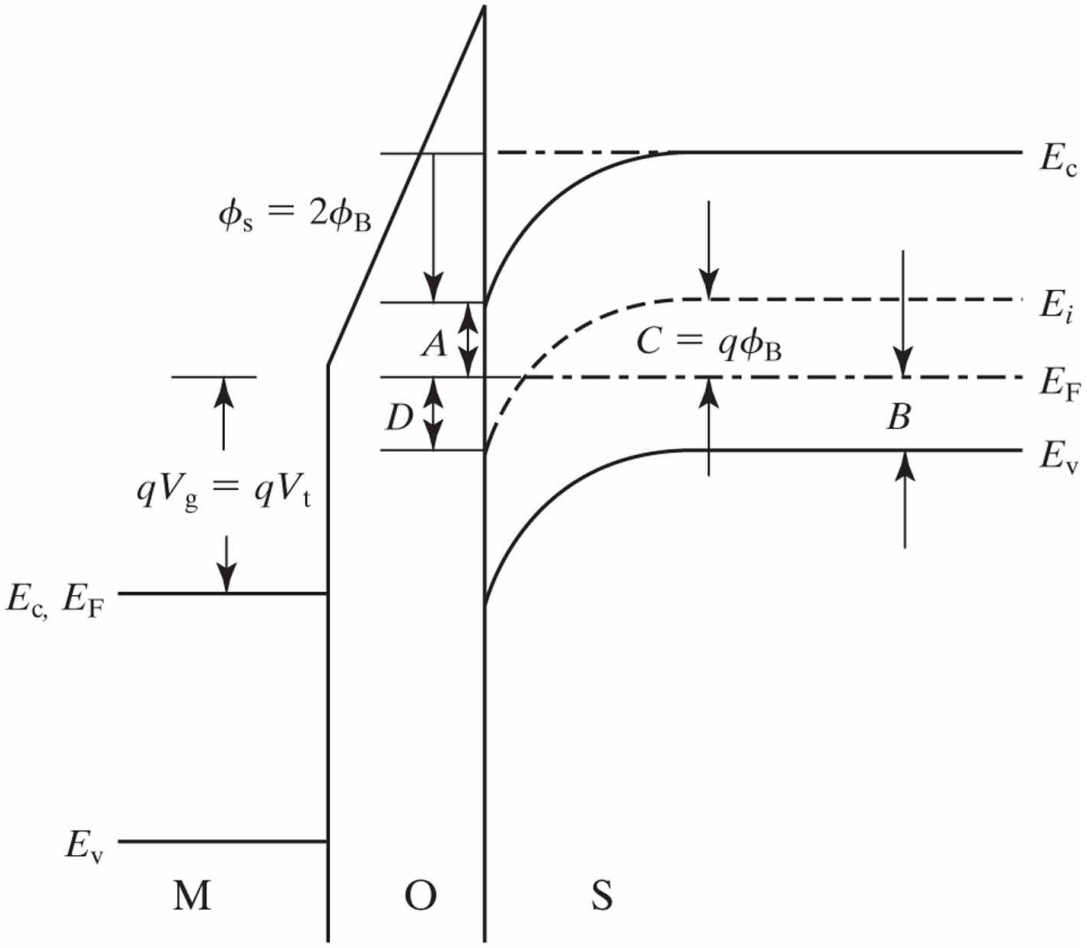

Figure 5.8 Theoretical threshold voltage vs. body doping concentration using Eq. (5.4.3). See Section 5.5.1 for a discussion of the gate doping type.

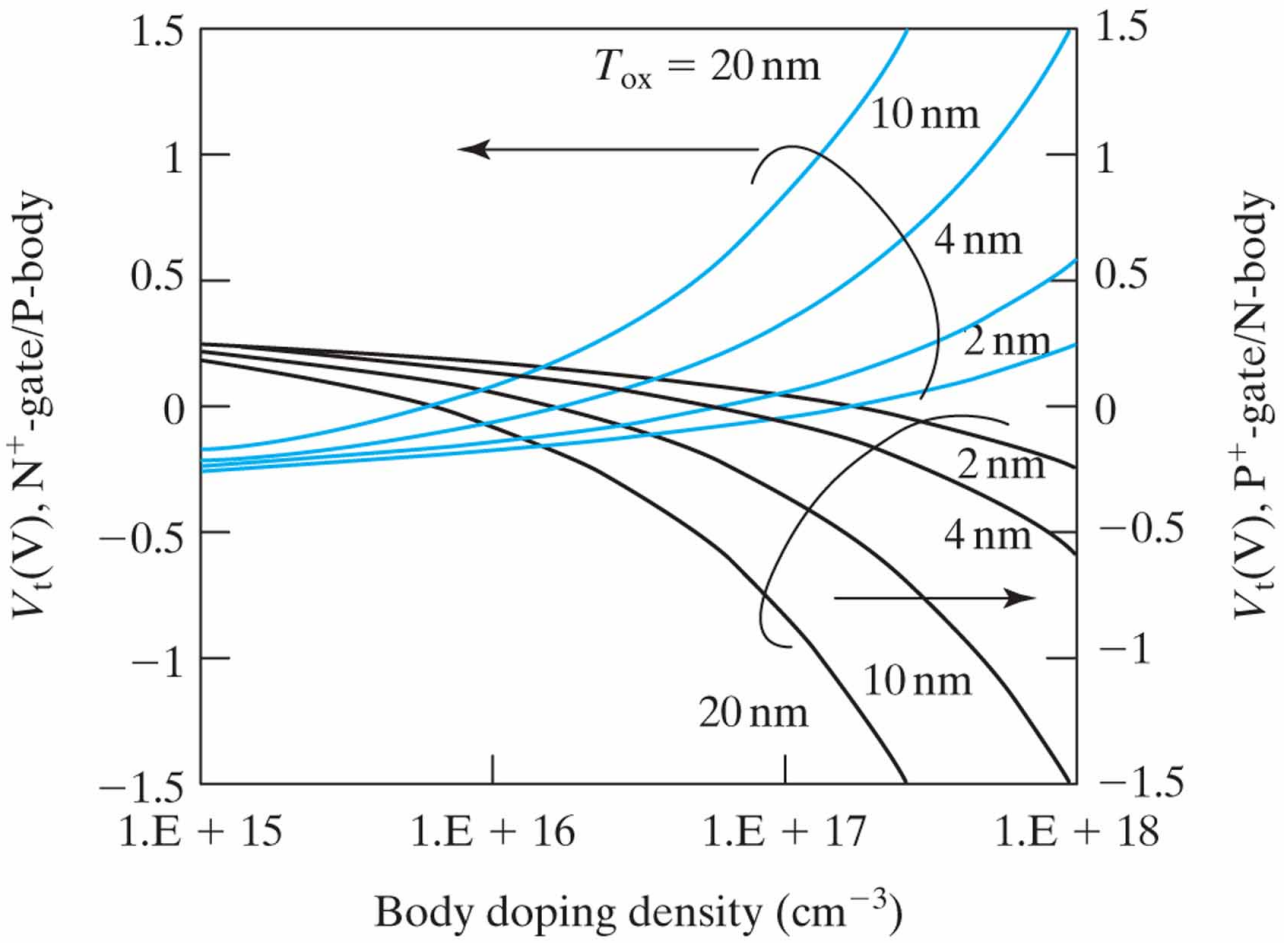

Figure 5.9 An MOS capacitor biased into inversion. (a) Types of charge present; (b) energy band diagram with arrow indicating the sense of positive V_g.

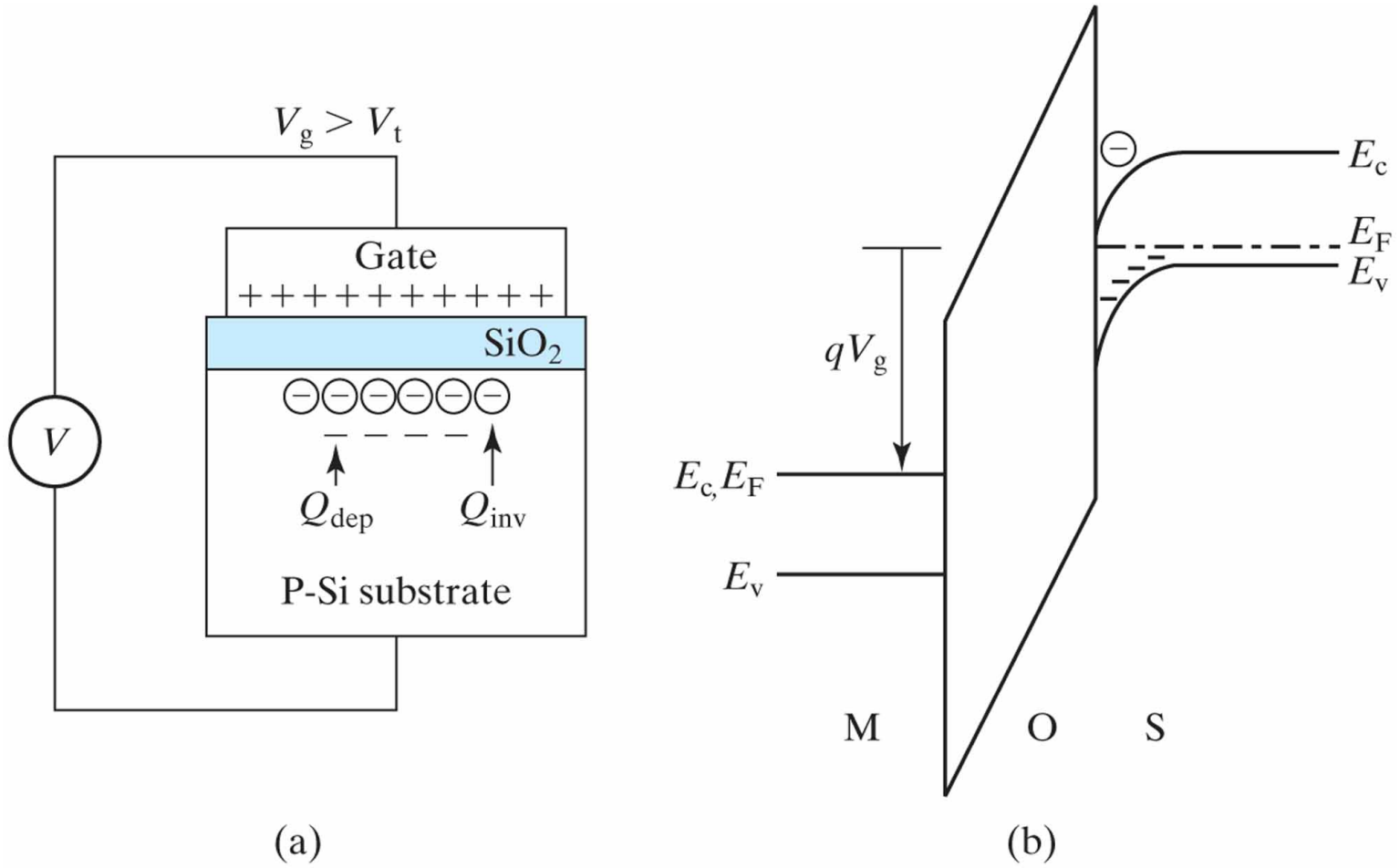

Figure 5.10 (a) The surface inversion behavior is best studied with a PN junction butting the MOS capacitor to supply the inversion charge. (b) The inversion layer may be thought of as a thin N-type layer.

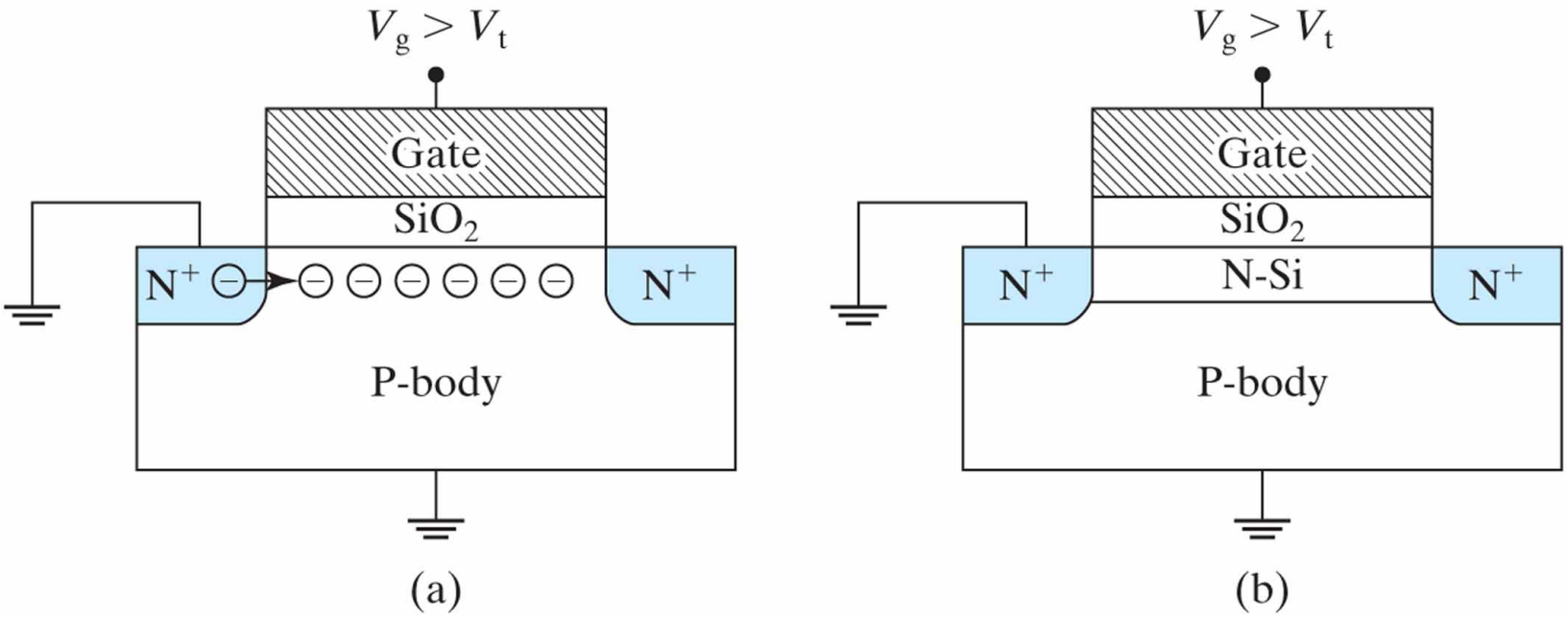

Figure 5.11 Surface potential saturates at $2\phi_B$ when V_g is larger than V_t.

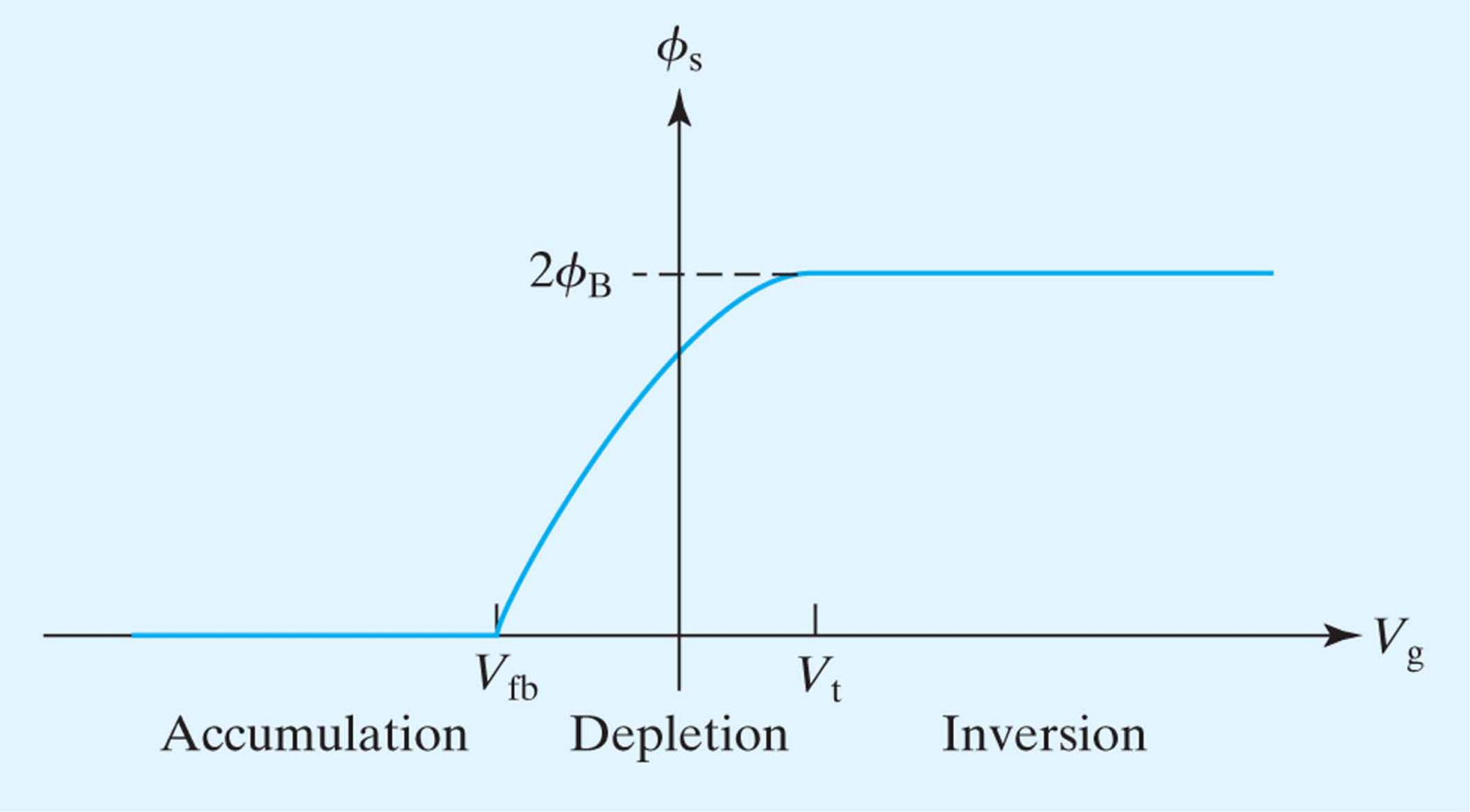

Figure 5.12 Depletion-region width in the body of an MOS capacitor.

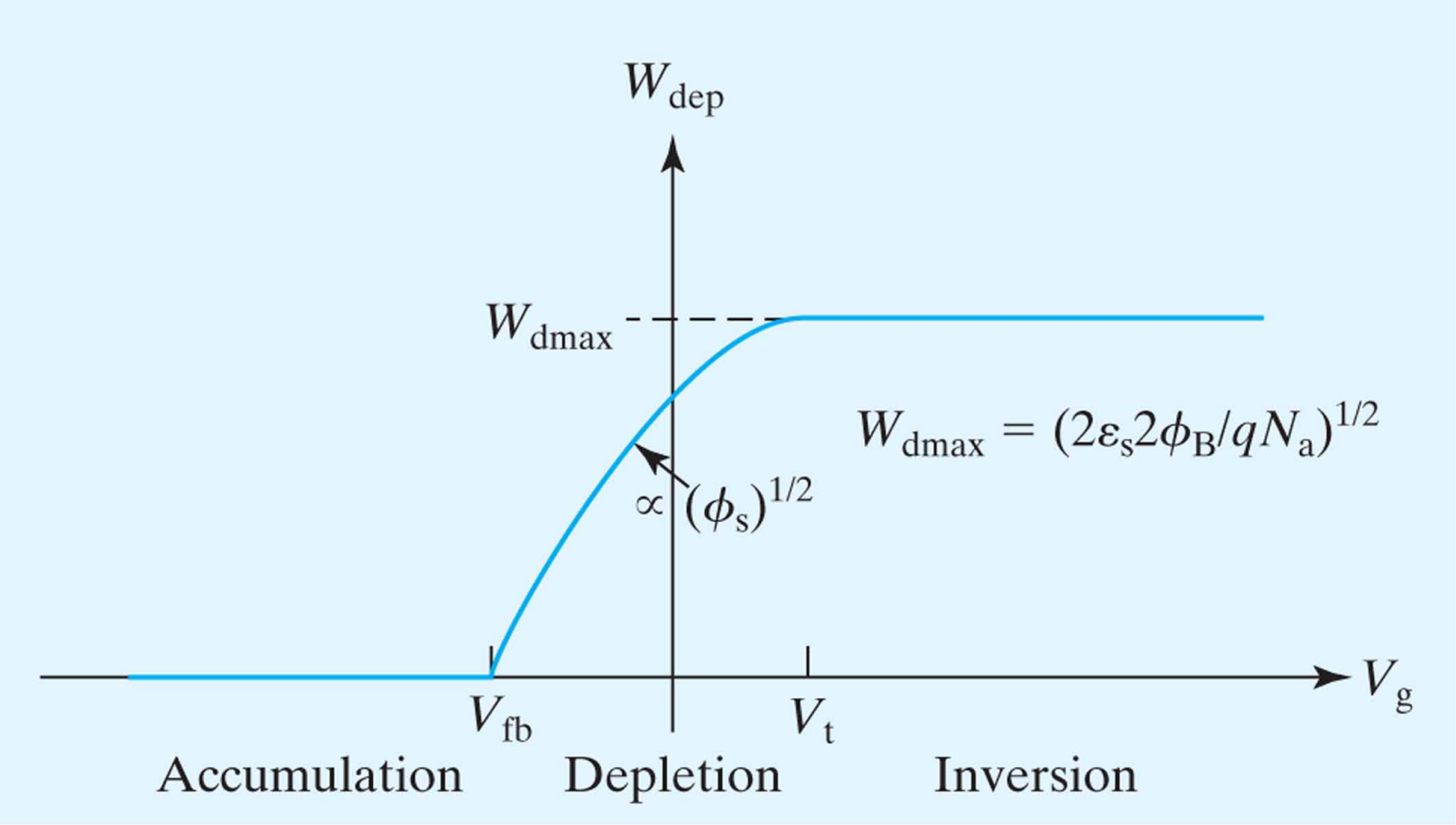

Figure 5.13 Components of charge (C/cm^2) in the MOS capacitor substrate: (a) depletion-layer charge; (b) inversion-layer charge; and (c) accumulation-layer charge.

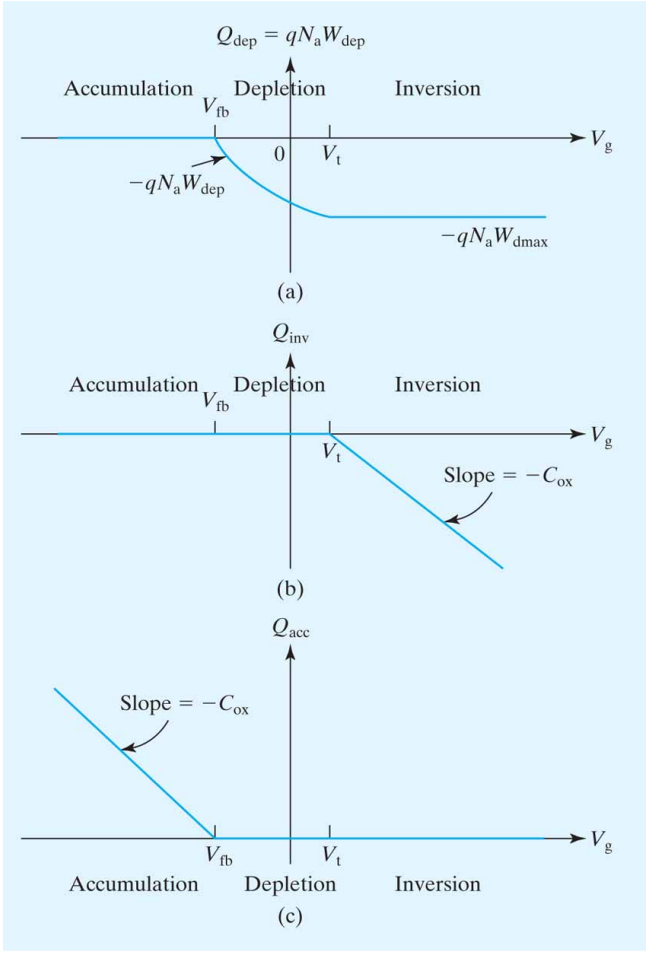

Figure 5.14 The total substrate charge, Q_{sub} (C/cm^2), is the sum of Q_{acc}, Q_{dep}, and Q_{inv}.

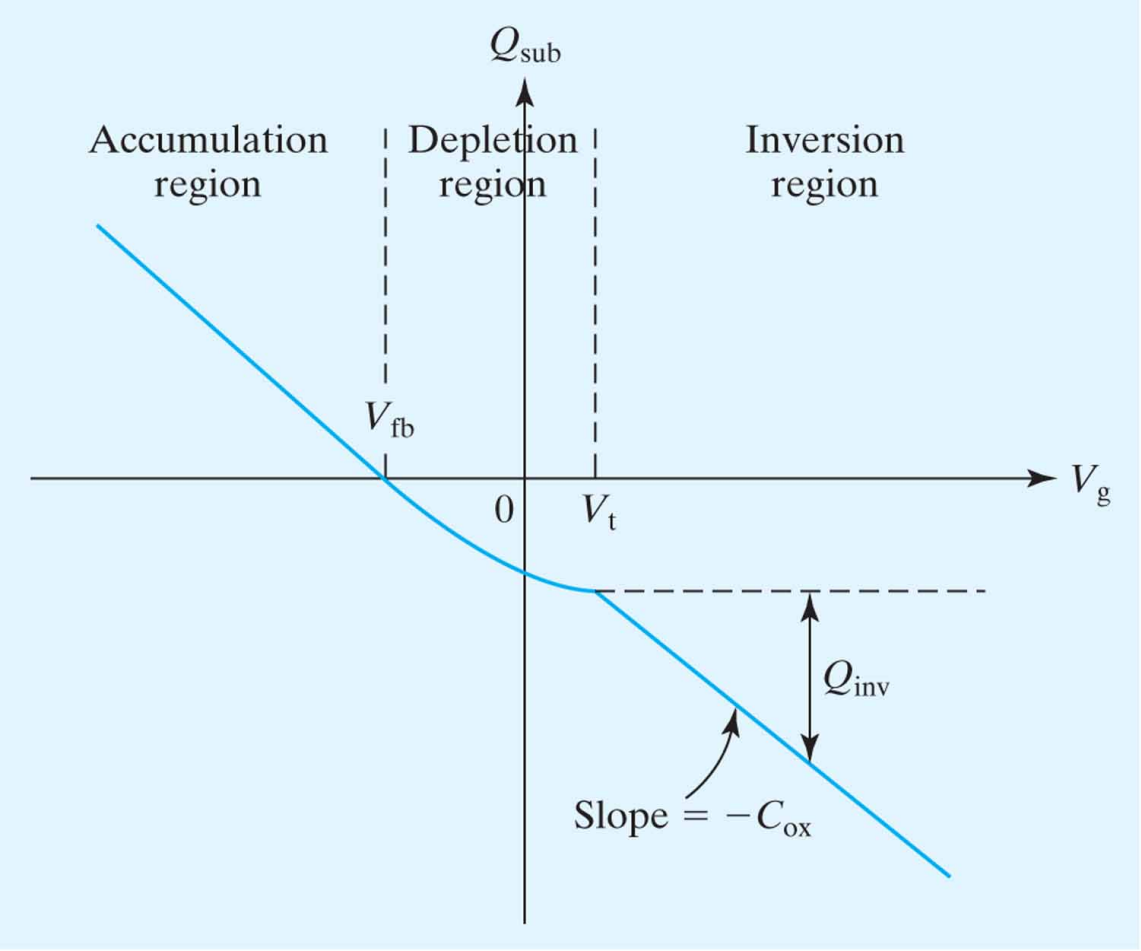

Figure 5.24 Average location of the inversion-layer electrons is about 15 Å below the Si–SiO_2 interface. Poly-Si gate depletion is also shown.

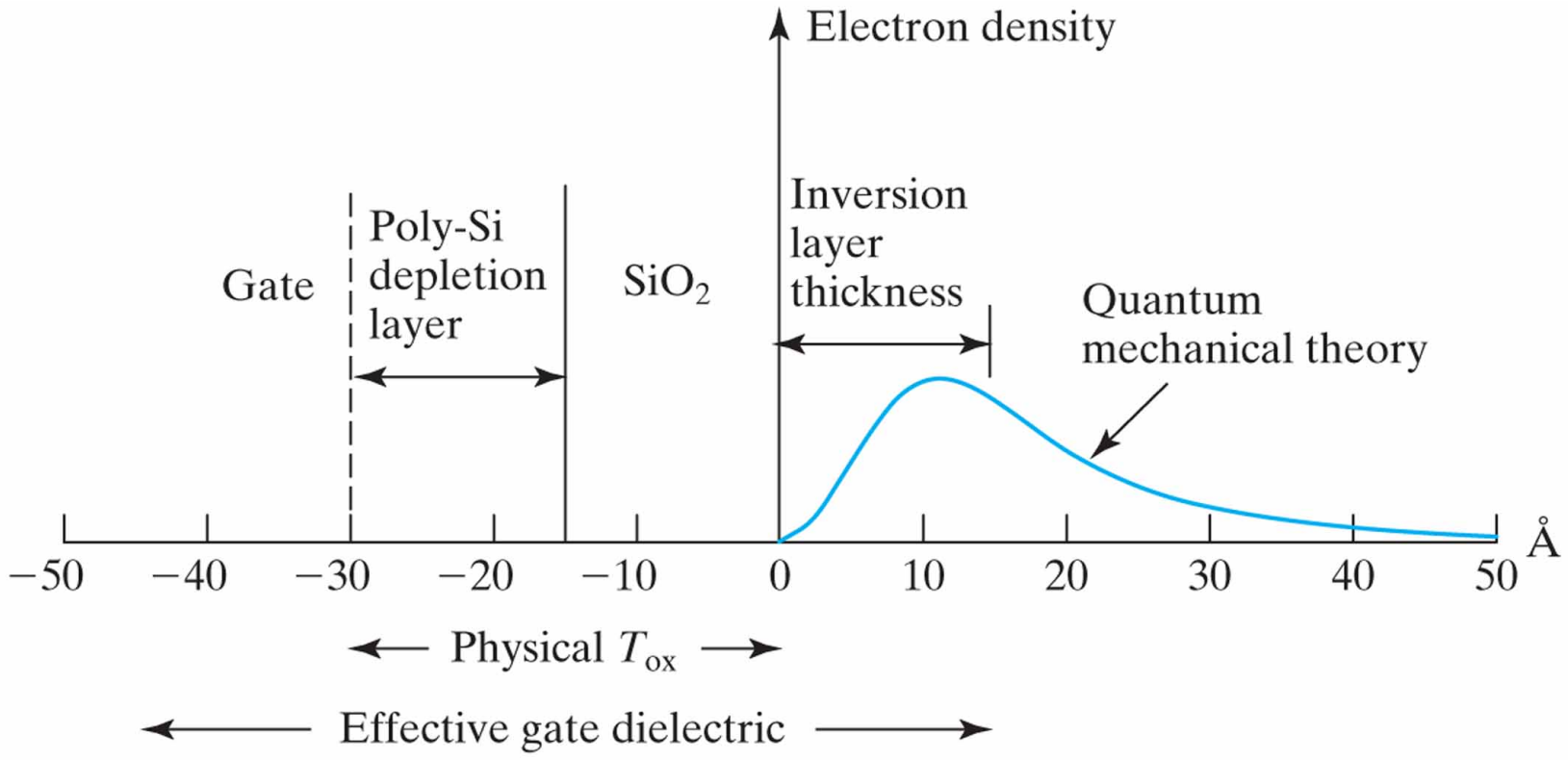

Figure 5.15 Setup for the C–V measurement.

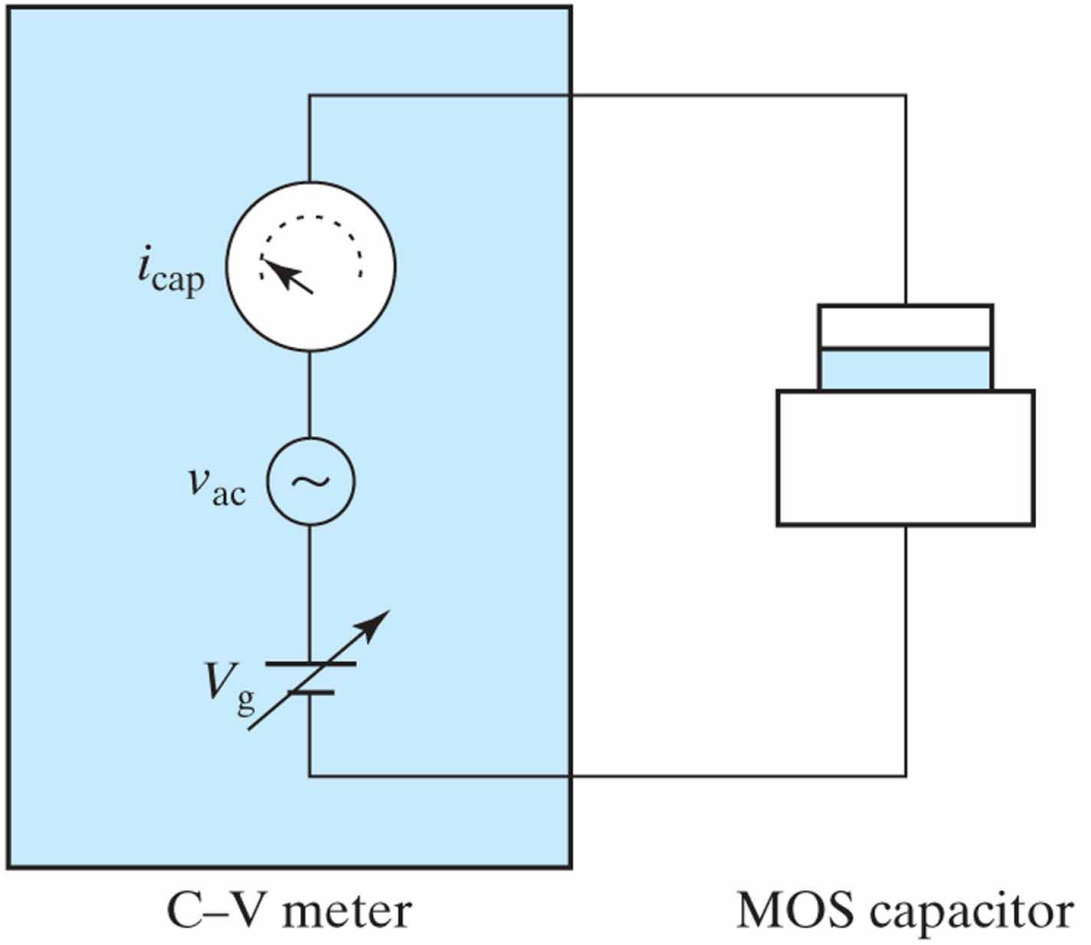

Figure 5.16 The quasi-static MOS C–V characteristics.

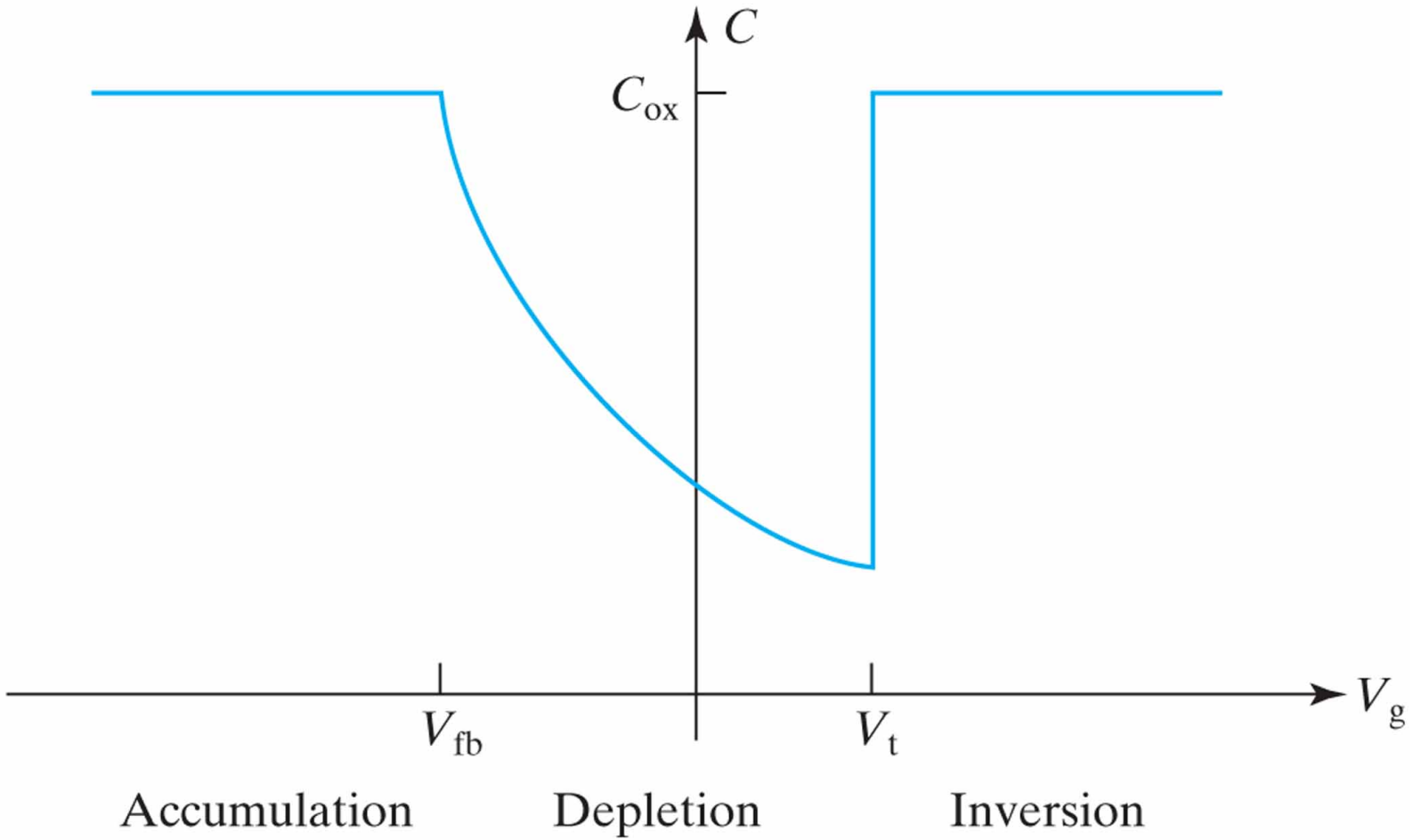

Figure 5.17 Illustration of the MOS capacitor in all bias regions with the depletion-layers shaded. (a) Accumulation region; (b) depletion region; (c) inversion region with efficient supply of inversion electrons from the N region corresponding to the transistor *C*–*V* or the quasi-static *C*–*V*; and (d) inversion region with no supply of inversion electrons (or weak supply by thermal generation) corresponding to the high-frequency capacitor *C*–*V* case.