# IH1611
# Laboratory Exercise
## Fall 2020

### Introduction

This laboratory exercise demonstrates electrical measurements of silicon and SiC based semiconductor devices (MOSFETS and pn-diodes) fabricated in the KTH cleanroom in Kista.

The main learning objectives are to:

- experimentally investigate the forward and reverse IV-characteristics of pn-junction (silicon and SiC diodes)
- fit simplified models of the pn-diode to real device data
- investigate the influence of ambient conditions, such as light (illumination) and temperature, on the diode characteristics
- extract physical parameters from the samples, in this case the doping level

At the end of the exercise, each student receives measurement data transferred by email/online. No USB memory sticks are allowed. These data should then be fitted by suitable models and the model parameters should be extracted.

### Preparation

A lab assistant will guide the students through the tasks and answer any questions. To prepare the students are recommended to read this lab instruction and Chapter 4 of Hu's book. Especially understanding chapter 4.4-4.9 is useful for preparation as well as for writing of the report.

### Measurement equipment

During the exercise the students will have access to a measurement station that will provide the possibility to measure the capacitance, or the current as a function of applied voltage for pn-diodes on a wafer (piece). The measurement station (or probe station) has a chuck where the wafer (piece) can be placed and measurement probes can be brought into contact with the diodes on the wafer. The probe station is also equipped with a microscope to localize the diodes on the wafer. The probes are connected to either a current-voltage (IV) parameter analyzer (alternatively a stand-alone SMU), or a capacitance-voltage (CV) meter. The voltage is swept and the current or the capacitance is recorded for every biasing point. The measured data is stored in a text-file and will be provided to the students.

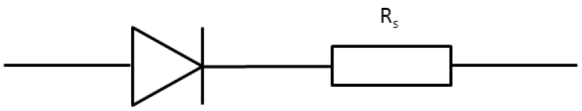
### IV model

The current-voltage characteristics of pn-diodes is often (for example in SPICE-models) modelled as:

$$I_D = I_O\left(exp\left(\frac{q(V - I_D R_S)}{nkT}\right)\right)$$

where $I_o$ is the reverse saturation current (see eq 4.9.5 in Hu's book), $V$ is the voltage over the pn-junction and $n$ is the ideality factor ($n$ = 1 if generation and recombination in the depletion region is negligible and $n$ = 2 if generation and recombination in the depletion layer determines the current).

To model any potential drop in the connections to the diode or in the p and n-regions of the diode a resistance is placed in series with the diode. A supplementary material has been attached to the end of this document with a worked out example showing the extraction of $R_S$.




## CV model

In the reverse direction the capacitance of the pn-diode is given by the depletion layer capacitance $C_{dep}=A\varepsilon_s/W_{dep}$ where $A$ is the area of the diode, $\varepsilon_s$ is dielectric constant of the semiconductor and $W_{dep}$ is the depletion layer width. The depletion layer width is a function of the applied reverse voltage (see Hu's chapter 4.3-4.4).

## Sample description

Silicon 100 mm (4 inch) wafer

A wafer with about 100 patterned dies including many teststructures has been prepared in the Electrum cleanroom. Measurements will be performed on $p^+n$ and $n^+p$ diodes. The diode area is 150×150 $\mu m^2$. The diodes are formed at the source-to-substrate junctions of large area NMOS or PMOS transistors.

Silicon carbide dies

A small piece of a silicon carbide wafer, also fabricated in the cleanroom, is provided. Measurements on diodes with different n- and p-type doping levels are possible.

## Report submission and criteria

For a pass the report should fulfill the criteria agreed upon during the first seminar. Each student should write an individual report. It is especially important that the report describes the methodology clearly so that student colleagues can understand the methodology and provide feedback on it. A clear comparison between the model characteristics and the measured characteristics is essential. By writing the report students are expected to practice writing a report and gain knowledge in how models can be used to describe semiconductor components and how model parameters can be extracted from real device data.

The reports are submitted online, under the assignments menu in the CANVAS LMS

The deadline is February 19, 23:59. All students will receive reports to read and provide feedback on. After receiving feedback at the feedback seminar scheduled on February 25, 15-17, a final version of the report should be submitted online before the second deadline, March 2, 23:59.

## List of Tasks

**Task 1, Use data from a $p^+n$ or an $n^+p$ diode to fit model parameters**

Determine the reverse saturation current $I_o$, the ideality factor $n$, and the series resistance $R_s$ of the diode. To complete this task you need to perform forward and reverse IV-sweeps with a suitable applied voltage range and enough steps (small voltage step).

**Task 2, Use data from a $p^+n$ diode to find substrate doping**

Determine the doping concentration $N_D$ from CV measurements. Before the CV-measurement estimate the maximum feasible reverse voltage by an IV measurement.

**Task 3, Investigate the influence of ambient conditions on the diode characteristics**

In this task both the silicon wafer and the SiC piece should be utilized. Perform reverse IV sweeps in dark and under illumination. (For the silicon wafer these measurements could be combined with **Task 1**). Perform measurements at room temperature and at least one selected elevated temperature, focus on the forward characteristics.